Design Example Report

Title	**26 W Multi Output Flyback Converter with Two CV and One CC Using InnoMux™ IMX111U and InnoSwitch™3-MX INN3465C**
Specification	90 VAC – 265 VAC Input; 5 V / 1 A, 12 V / 420 mA and 32 V – 40 V / 400 mA Outputs
Application	LED Monitor, TV, White Goods
Author	Applications Engineering Department
Document Numl	DER-871
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Summary and Features

Unique single-stage conversion, multiple-output, flyback architecture enabling:

- High efficiency across the universal line range
- High regulation accuracy - independently regulated 5 V / 1 A and 12 V / 0.42 A CV outputs with extremely fast load transient response of 150 μs and 250 μs respectively
- One CC (LED) output with wide string voltage range of 32 V to 40 V
- Configurable for
    - Analog dimming mode
    - Straight PWM dimming mode
    - Filtered PWM dimming mode and
    - Hybrid dimming mode.
- Safety features
    - Output overvoltage protection (OVP), eliminating the need for a fault protection optocoupler
    - Output power limit set independently for each output
    - Accurate thermal protection with hysteretic shutdown
    - Input voltage monitor with accurate brown-in/brown-out and overvoltage protection

InnoSwitch3-MX and InnoMux form the industry first AC/DC chipset with isolated, safety-rated integrated feedback. In addition, there is built-in synchronous rectification for increased efficiency.

The control chipset incorporates isolated feedback and communication channels, combining all the benefits of secondary-side control with the simplicity of primary-side regulation.

The new architecture achieves tight cross regulation across multiple outputs and high overall efficiency while simplifying the overall system by obviating the need for post-regulation. The single-stage converter reduces board size significantly and reduces the part count compared to the equivalent conventional converter based on multiple conversion stage topology.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a Switch Mode Power Supply (SMPS) intended for appliance applications. The SMPS, utilizes the Power Integration's InnoSwitch3-MX/InnoMux control chip set. The chip set implements a multiplexing power control algorithm, where the energy stored in the primary winding of the transformer during any primary conduction interval is subsequently delivered to only one of the converter's main outputs (CV1, CV2 or LED). More specifically, this is achieved by controlling the state of the switches SW1 and SW2 (Figure 1) during the flyback interval of each switching cycle. Utilizing a single magnetic component (transformer TX 1), the controller directs the energy flow as needed to all outputs based on respective loading requirements, thus keeping each output accurately controlled. If the energy pulse needs to be delivered to the CV1 output, SW1 is turned ON prior to the end of the primary conduction interval while SW2 is kept off. Similarly, for CV2, the SW2 is turned on, but SW1 is OFF. Otherwise if SW1 and SW2 are both OFF, the energy is delivered to the LED output via the rectification diode D1.

The SMPS has two Constant Voltage (CV) outputs, 5 V / 1 A and 12 V / 0.42 A and a single Constant Current (CC) output, capable of delivering maximum of 0.4 A current into an LED stack with voltage from 32 V to 40 V. The current through the LED stack is controlled from zero to maximum by an analog dimming signal (ADIM) with a full scale (FS) of 1.5 V. The Power Supply Unit (PSU) can deliver total maximum continuous output power of 26 W, with universal mains input (from 90 VAC to 265 VAC).

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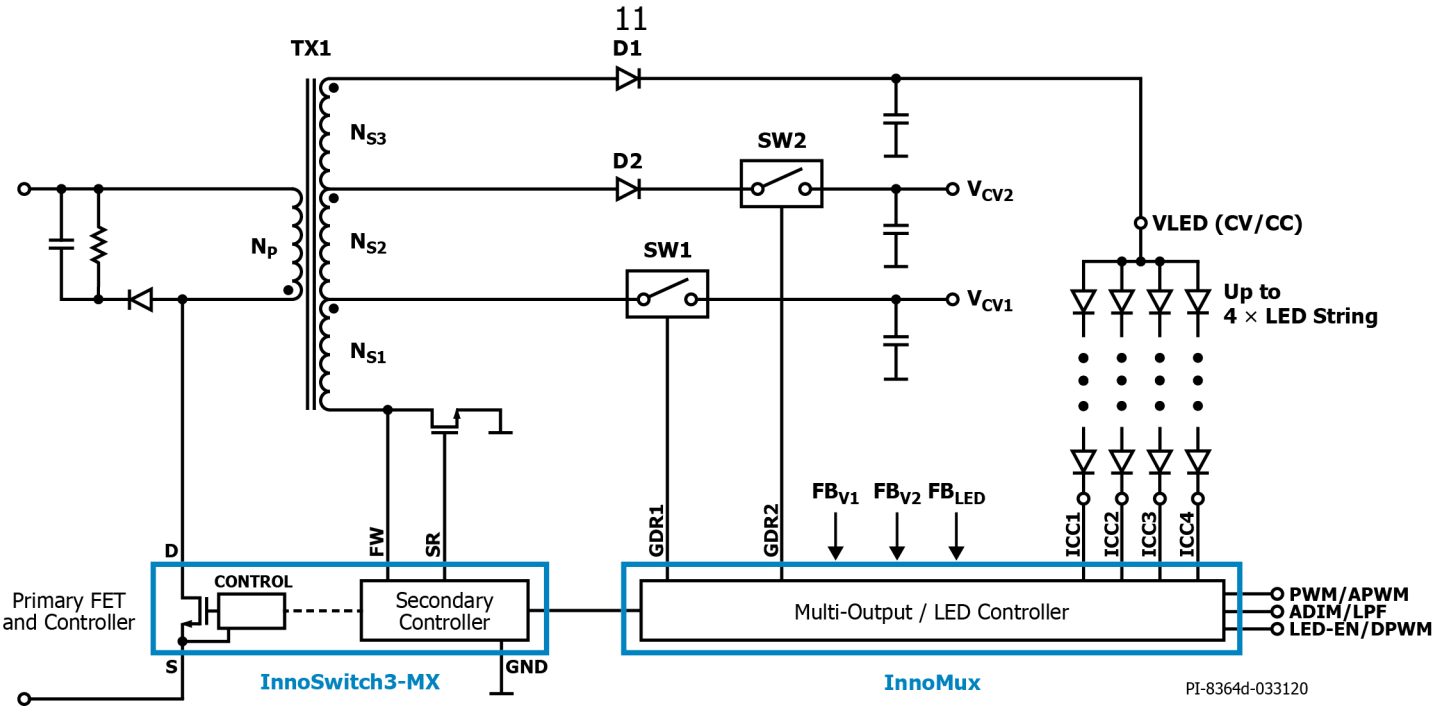

Figure 1 – DER-871 High Level Schematic.

The feedback (FB) pins FB_{V1}, FB_{V2} and FB_{LED} continuously sense the output voltages. If the voltage of any of the outputs drops below regulation level, the multi-output controller InnoMux sends a request for pulse to secondary controller of the InnoSwitch3-MX. This type of pulse-by-pulse regulation results in quick response and excellent cross regulation. For the described multiplexing algorithm to work correctly, it is essential that the reflected voltage of each winding must be higher than that of the preceding lower output voltage winding in order to effectively steer the power:

$$\frac{V_{CV1}}{N_{S1}} < \frac{V_{CV2}}{N_{S1}+N_{S2}} < \frac{V_{LED}}{N_{S1}+N_{S2}+N_{S3}}$$

Transformer with stacked or independent secondaries may be used as appropriate. The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. The actual performance is illustrated in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	3 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	±5%.
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0		1	A	
Output Voltage 2	V_{OUT2}	11.4	12	12.6	V	±5%.
Output Ripple Voltage 2	$V_{RIPPLE2}$			100	mV	20 MHz Bandwidth.
Output Current 2	I_{OUT2}	0		0.42	A	
Output Voltage 3	V_{OUT3}	32	40	45	V	
Output Ripple Current 3	$I_{RIPPLE3}$			40	mA	20 MHz Bandwidth.
Output Current 3	I_{OUT3}	0	0.4	0.45		
Total Output Power						
Continuous Output Power	P_{OUT}			26	W	
Efficiency						
Full Load	η	87			%	Measured at 110 / 230 VAC, POUT 25 ºC.
No-Load Input Power				<0.3	W	Measured at 230 VAC 25 ºC, 5 V 20 mA, STDBY Pin Pulled Low.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge Common Mode Ring Wave		4		6	kV	100 kHz Ring Wave, 12 Ω Common Mode.
Surge Combination Wave				1	kV	Combination Wave, 2 Ω Differential Mode.
ESD		±2		±15	kV	Air Discharge.
		±2		±8		Contact Discharge.
Ambient Temperature	T_{AMB}	0		60	ºC	Free Convection, Sea Level.

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3 Schematic

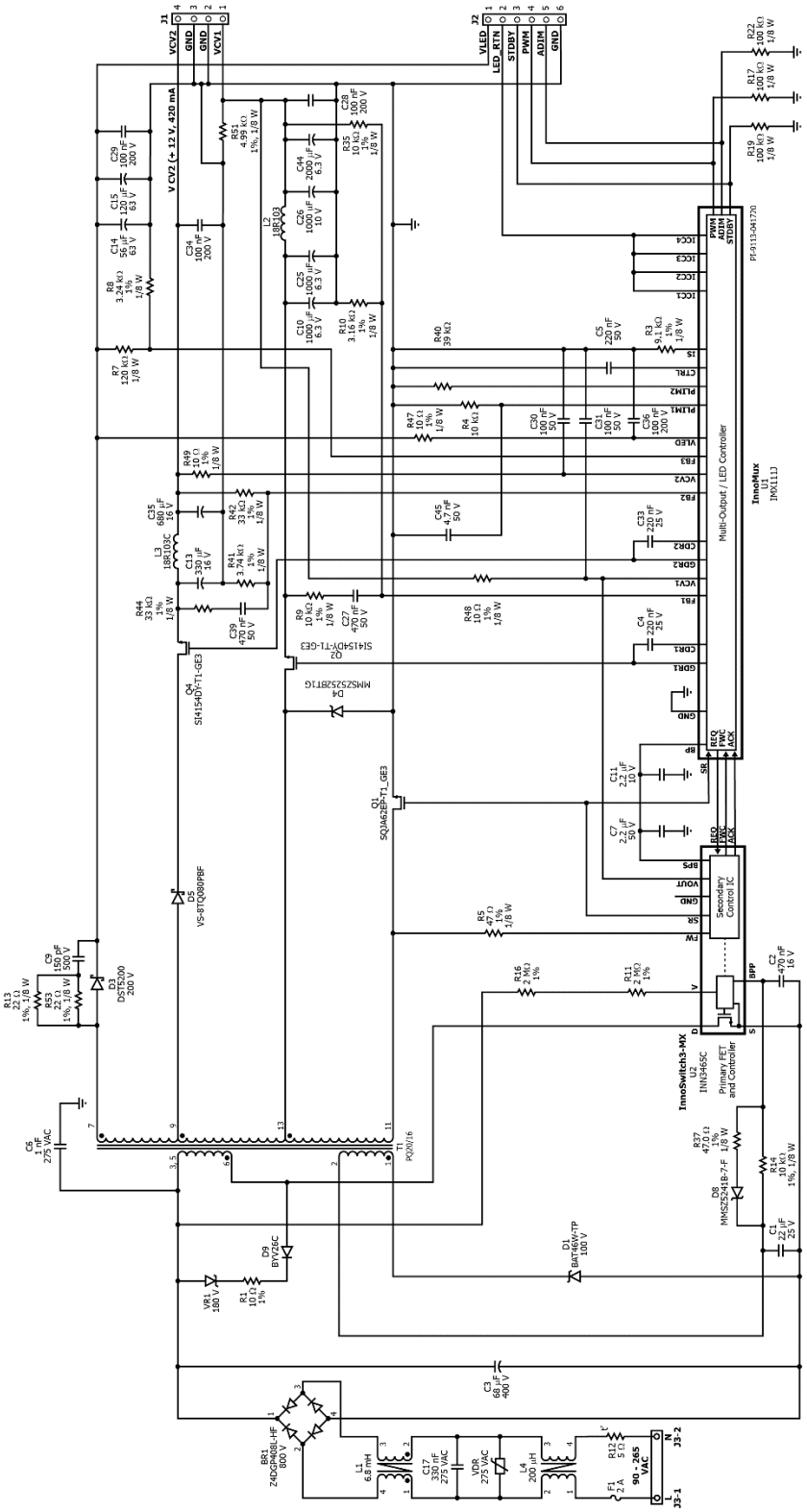

Figure 2 – Schematic.

4 Bill of Materials

The total number of parts fitted in DER-871 is 60 with a total number of positions of 78.

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	RECT BRIDGE, 800V, 4A	Z4DGP408L-HF	Comchip Tec
2	1	C1	22 μF, 25 V, Ceramic X5R, 1206	CL31A226KAHNNNE	Samsung
3	1	C10	1000 μF, 6.3 V, Polymer	RL80J102MDN1KX	Nichicon
4	1	C11	2.2 μF, 10 V, Ceramic, 0805	C0805C225M8RACTU	Kemet
5	1	C13	330 μF, 16 V, Polymer	RL81C331MDN1	Nichicon
6	1	C14	56 μF, 63 V, Polymer	RNU1J560MDN1PH	Nichicon
7	1	C15	120 μF, 63 V, Electrolytic	EKZE630EC3121MH20D	United Chemi-con
8	1	C17	330 nF, 275 V_{AC}, Film, X2	ECQ-U2A334ML	Panasonic
9	1	C2	470 nF, 16 V, Ceramic, 0805	CC0805KKX7R7BB474	Yageo
10	1	C26	1000 μF, 10 V, Electrolytic	UHE1A102MPD6	Nichicon
11	2	C27 C39	470 nF, 50 V, Ceramic, 0805	GRM21BR71H474KA88L	Murata
12	4	C28, C29, C34, C36	100 nF, 200 V, Ceramic, 1206	VJ1206Y104KXCAT	Vishay
13	1	C3	68 μF, 400 V, Electrolytic	EEU-EE2G680	Panasonic
14	2	C30 C31	100 nF, 50V, Ceramic, X7R,0805	CC0805KRX7R9BB10	Yageo
15	1	C35	680 μF, 16 V, Electrolytic	EKZE160ELL681MH20D	United Chemi-con
16	2	C4 C33	220 nF, 25 V, Ceramic, X7R, 0805	CC0805KRX7R8BB224	Yageo
17	1	C5	220 nF, 50 V, Ceramic, X7R,0805	GRM21BR71H224KA0	Murata
18	1	C6	1 nF, 250V_{AC}, Ceramic, Y1	440LD10-R	Vishay
19	1	C7	2.2 μF, 50 V, Ceramic, X7R, 1206	CL31B225KBHNNNE	Samsung
20	1	C9	150 pF, 500V, Ceramic, 0805	CC0805JRNPOBBN151	Yageo
21	1	C44	2000 μF, 6.3V, Electrolytic, Low ESR 30 mΩ	EEUFS0J202L	Panasonic
22	1	J3	Term Block 5.08 mm 2Pos	ED120/2DS	On Shore Tec
23	1	D1	Diode, Schottky, 100V, 0.075A, SOD123	BAT46W-TP	Micro Commercial
24	1	D3	200 V, 5 A, Diode, Schottky, TO-220AC	DST5200	Littelfuse
25	1	D4	Diode Zener, 24 V, 500 mW, SOD123	MMSZ5252BT1G	ON Semi
26	1	D5	80 V, 8 A, Diode, Schottky, TO-220AC	VS-8TQ080PBF	Vishay
27	1	D8	Diode Zener, 11 V, 500 mW, SOD123	MMSZ5241B-7-F	Diodes
28	1	D9	600 V, 1 A, Ultrafast Recovery, SOD57	BYV26C	Vishay
29	1	F1	2 A, 250 V, Slow, TR5	37212000411	Littelfuse
30	1	J1	4 Positions (1 x 4) Header	DF1B-4P-2.5DSA(01)	Hirose
31	1	J2	6 Positions (1 x 6) Header	DF1B-6P-2.5DSA(01)	Hirose
32	1	JP1 / R12	5Ω, NTC, Radial 9.5mm	B57235S0509M051	TDK
33	1	L1	CMC, 6.8mH @ 10kHz 1.3A, 2 Line	B82731M2132A030	TDK
34	2	L2 L3	10 μH, 3.45A, Inductor	18R103C	Murata
35	1	L4	CMC, 200uH @ 100 kHz, 0.4A, 2 Line	32-00315-00	Power Integrations
36	1	Q1	N-Fet, 60 V, 60 A, PowerPAK SO-8	SQJA62EP-T1_GE3	Vishay
37	2	Q2 Q4	N-Fet, 40 V, 36 A, 8-SO	SI4154DY-T1-GE3	Vishay
38	1	R1	RES, 10 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic
39	1	R10	RES, 3.16 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3161V	Panasonic
40	2	R11 R16	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
41	2	R13 R53	RES, 22 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF22R0V	Panasonic
42	3	R17 R19 R22	RES, 100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
43	1	R3	RES, 9.1 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF9101V	Panasonic
44	1	R4	RES, 10 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ103V	Panasonic
45	1	R40	RES, 39 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ393V	Panasonic
46	1	R41	RES, 3.74 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3741V	Panasonic
47	2	R42 R44	RES, 33 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3302V	Panasonic
48	3	R47 R48 R49	RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
49	2	R5 R37	RES, 47.0 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic
50	1	R51	RES, 4.99 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4991V	Panasonic
51	1	R7	RES, 120 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1203V	Panasonic

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52	1	R8	RES, 3.24 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3241V	Panasonic
53	3	R9 R14 R35	RES, 10 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
54	1	T1	PQ20-16, Vertical, 14 pins, DER-871_26W_A1	Der871_26W_A1	Power Integrations
55	1	U1	InnoMux Master	IMX111J	Power Integrations
56	1	U2	InnoSwitch3-MX	INN3465C	Power Integrations
57	1	VDR	275 VAC, 45 J, 10 mm, Radial	V275LA10P	Littlefuse
58	1	VR1	180 V, 3 W, TVS, SMB	1SMB5955B	ON Semi
59	1	C25	1000 μF, 6.3 V, Polymer	RL80J102MDN1KX	Nichicon
60	1	C45	4.7 nF, 50 V, Ceramic, X7R, 1206	CC1206KRX7R9BB472	Yageo

5 PCB Assembly

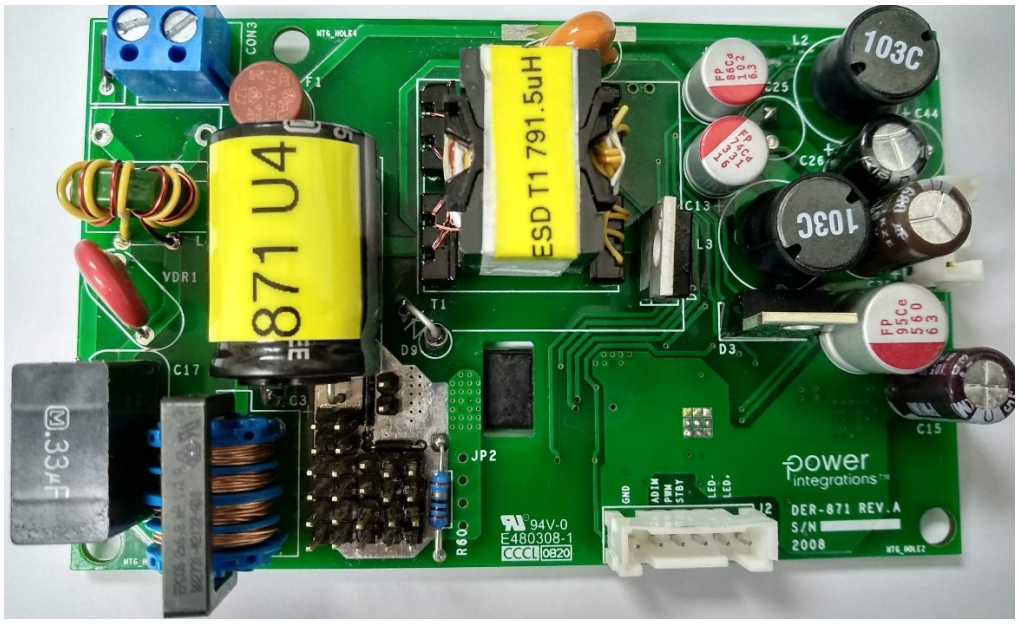

Figure 3 – PCB, Top View.

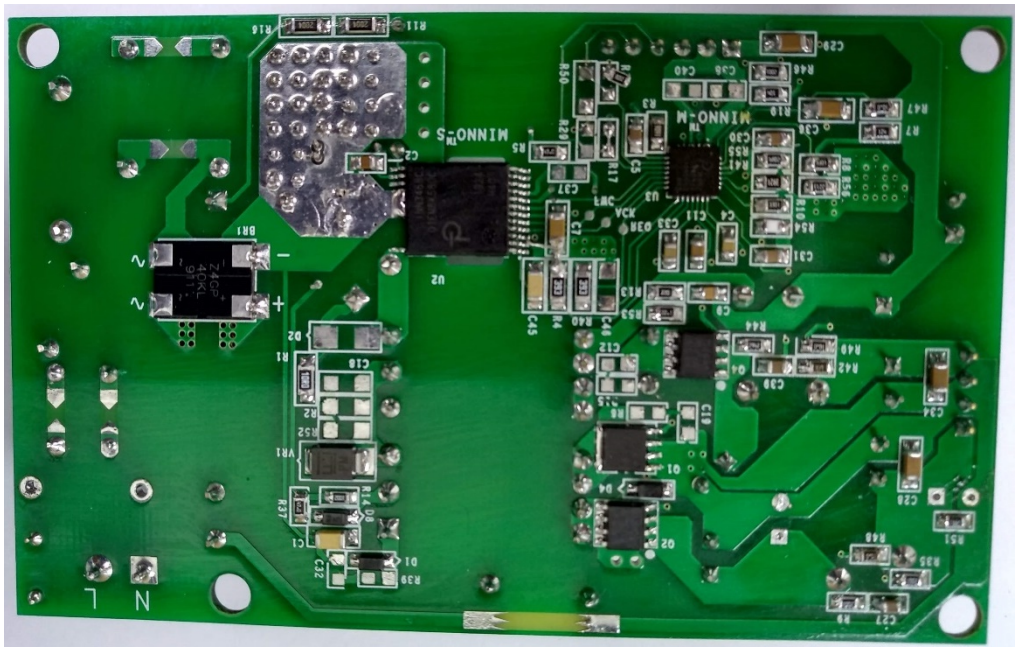

Figure 4 – PCB, Bottom View.

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6 Circuit Description

6.1 *Input Rectifier and EMI Filter*

A two-stage EMI filter is used: C17/L1 - for the lower frequency range and L4/C41 for the high frequency range. Mainly common mode noise is suppressed by the input EMI filter, but some degree of differential noise attenuation is also achieved. These measures along with the Y capacitor C6 and the screen windings in the transformer keep the conducted emissions below the specification limits.

The bulk storage capacitor C3 provides DC voltage smoothing after the bridge rectifier BR1. VDR1 provides protection against differential voltage surges. Resistor R12 (NTC) limits the inrush current on power up. Fuse F1 protects the PSU from drawing excessive current from the mains.

6.2 *Primary-Side*

6.2.1 Primary Switch Arrangements

The transformer primary is connected between the input DC bus (VIN_DC+) and the drain D of the integrated primary switch of InnoSwitch3-MX (U2 pin 24). Primary current loop closes to the negative terminal of C3 via the S pin (tab) of U2 (pin 16). A Zener type primary clamp (R1, VR1, D9) is used to limit the peak drain voltage of the integrated primary switch, due to the effects of transformer leakage inductance and output trace inductance.

6.2.2 Primary-Side Controller Power Source and OVP Protection

The primary-side controller is part of the InnoSwitch3-MX (U2). It is self-starting, using an internal high-voltage current source to charge the BPP capacitor C2, when AC voltage is first applied to the converter input. During normal operation (steady-state) the primary-side of the controller is powered from an auxiliary winding on the main transformer. The voltage across this winding is rectified and filtered using diode D1 and capacitor C1, and then connected to the BPP pin via a current limiting resistor R14.

6.2.3 Primary-Side OVP, Brown-In and Brown-Out Protection

A crude primary-side output overvoltage protection (OVP) is implemented by Zener diode D8 and the series resistor R37. In the event of an uncontrolled overvoltage at the output, the increased voltage at the bias winding causes the Zener diode D8 to break into conduction, increasing the current into the BPP pin. If this current exceeds a predetermined value I_{SD} = 8.9 mA, the OVP protection is triggered and the controlled implements a latch-off shut down.

Resistor R16 and R11 provide line voltage sensing to facilitate controlled brown-in/out transients. The thresholds for these transients are set to approximately 75 VAC and 65 VAC respectively. At approximately 320 VAC, the current through these resistors exceeds the input over overvoltage threshold, which results in the disabling of U2.

6.2.4 Primary Peak Current Limit

The value of capacitor C2 is used to set the maximum primary current to STANDARD or to INCREASED level. In this case 0.47 μF capacitance sets the primary-side controller peak current limit to its STANDARD level of 1.15 A.

6.3 *Secondary-Side*

The secondary-side of the InnoSwitch3-MX (U2) is powered from the 5 V BP rail generated internally in the InnoMux controller (U1 pin 19). Capacitor C7 is a local decoupling capacitor.

6.3.1 Primary to Secondary-Side Communication

The secondary-side of the InnoSwitch3-MX (U2) sends a request to the primary-side controller to initiate a switching cycle, by sending a pulse via the internal FluxLink, a galvanically isolated communication channel. This occurs when the InnoMux (U1) raises the REQ pin (U2 pin 1) above certain level.

6.3.2 Synchronous Rectifier (SR) FET Control

The SR FET (Q1) is gated on at the beginning of each flyback interval. In discontinuous current mode (DCM), the SR FET (Q1) is turned off when the voltage drop across its enhanced channel falls below certain threshold ($V_{SR(TH)}$). In continuous conduction mode (CCM), the SR FET (Q1) is turned off just prior to the secondary-side controller requesting a new switching cycle from the primary. This ensures that the primary switch and the SR FET are not turned on in the same time. The timing described above is synchronized by the waveform on the FW pin (9) of the secondary controller. The SR FET gate drive signal (U2 pin 7) has an amplitude of 5 V. Consequently, a logic level MOSFET must be used as a SR.

6.3.3 InnoSwitch3-MX to InnoMux Communication

Communication between the InnoSwitch3-MX secondary and the InnoMux controller (U1) is implemented through the following communication lines:

REQ (request) – this is an analog multi-level i/o line with the following thresholds:

- <0.3 V – InnoMux is in reset
- 0.3 V - 0.61 V – InnoMux is in idle ring measurement window mode
- 0.61 V - 1.22 V – no pulse requested, but InnoMux has control
- 1.22 V - 2.44 V – pulse requested
- >2.44 V – error, output over-voltage. Primary will be latched off.

ACK (acknowledge) – On recognition of request for switching cycle from the InnoMux controller, the InnoSwitch3-MX secondary control circuit sends an acknowledge pulse back to the InnoMux controller. This is a digital i/o line.

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The SR pin of the InnoSwitch3-MX drives the SR FET gate. It is also connected to the InnoMux SR pin. This communication line is used to informs InnoMux when the transformer is delivering energy to the secondary-side of the converter.

FWC (forward) – this is an indication of the total secondary discharge time. This is a digital signal from InnoSwitch3-MX to InnoMux. Similar to the SR signal, this signal indicates the flyback time more completely, as the SR may be turned off early.

6.3.4 InnoMux Power Supply

During start-up the InnoMux controller is powered from +V_LED via R47. There is a local decoupling capacitor C36 connected close to the VLED pin of U2. R47 and C36 are optional and provide additional ESD protection. An internal regulator reduces the +V_LED voltage to 5 V and outputs it to the BP bus (U1 pin 19). The InnoSwitch3-MX secondary-side circuitry is also powered from the BP rail. Capacitor C11 provides local decoupling for U1.

In steady-state the voltage on VCV2 (U1 pin 25) exceeds $VCV2_{MIN}$ (5.8 V to 8.0 V). The internal BP regulator input is switched from VLED to VCV2 pin to reduce power dissipation in the regulator. Resistor R49 and C30 are optional. They provide local decoupling as well as ESD protection.

6.3.5 Selection MOSFETs Drive

The gate drive amplitude for the selection MOSFETs Q2 and Q4 is approximately equal to the voltage on the BP rail (5 V). Consequently, logic level MOSFETs are used. Capacitors C4 and C33 are charged up to the level of the BP rail (5 V) from the DR1 and the DR2 pins respectively to GND. When a selection MOSFET needs to be gated on the corresponding capacitor, (C4 or C33) is referenced to the output rail (VCV1 or VCV2) through the CRD1 and CRD2 pins respectively.

The secondary control circuit in InnoSwitch3-MX needs access to the idle ring waveform in order to calculate the its timing and facilitate valley switching. Such access is ensured through the FW pin by keeping Q2 on after the secondary conduction time has expired.

6.3.6 Output Control

Output rectification for the CV1 output is provided by the SR FET (Q1) and the CV1 selection MOSFET (Q2). A Π – type LC filter (C10, C25, C26, C28, C44 and L2) ensures low output ripple voltage. The first stage filter capacitors C10, C25 have low ESR to minimize the switching noise. Capacitor C26 and C44 are Al-electrolytic type. Small multilayer ceramic (MLC) capacitor C28 is connected across the CV1 output terminals and provide low impedance bypass for any high frequency noise components. Output rectification for the CV2 output is provided by the SR FET (Q1), the CV2 selection MOSFET (Q4) and CV2 diode (D5). The filtering arrangement is similar to that of the CV1 output. It includes C13, C35, C49, C34 and L3.

Output rectification for the LED output is provided by SR FET (Q1) and diode (D3). A simple capacitive filter C14, C15 is used to provide energy storage and filtering at the LED output.

The RC snubber network R13, R53 and C9 damps high-frequency ringing across the rectifier diode D3 due to the transformer leakage inductance and the secondary's trace inductance oscillating with the diode capacitance.

Zener diode D4 is used as a voltage clamp for the transformer CV1 winding while the primary MOSFET is ON and Q1, Q2 and Q4 are turned off, and D5, D3 are reverse biased. In this condition, the secondary windings are floating with respect to GND. Without D4, the voltage on Q2 drain could be too high due to transformer winding capacitance interactions.

When the selection MOSFET (Q2) and the SR FET (Q1) are turned on, the transformer secondary windings are designed such that the voltage on the anode of D3 or D5 is below the lowest working LED string voltage and 12 V respectively. Therefore, D3 and D5 will remain reverse biased and all the transformer energy is directed to the CV1 output via Q1.

When the Selection MOSFET (Q2) is turned off and the Selection MOSFET (Q4) and SR FET (Q1) is turned on, the voltage on the anode of D3 is below the lowest working LED string voltage, keeping the diode reverse biased. In this condition the entire transformer energy is directed to the 12 V output.

When the Selection MOSFETs (Q2 and Q4) are turned off, and the SR FET (Q2) is turned on, the voltage on the anode of D3 rises until it is forward biased. In this condition, all the transformer energy is directed to the LED output.

The set point for the CV1 output +V_CV1 is determined by the potential divider R35, R10, which provide a feedback signal to the FB1 pin of InnoMux. Resistor R9 and C27 are loop compensation components. Similarly, the set point for the CV2 output +V_CV2 is determined by the potential divider R41, R42 which provide a feedback signal to the FB2 pin of InnoMux. R44 and C39 are loop compensation components.

+V_LED output overvoltage limit is set by R7 and R8 to FB3 (U1 pin 26). In this design it has been set to 55.7 V. Note that the actual +V_LED voltage is not set by these resistors and it varies depending on the LED stack voltage and the voltage across the LED drivers ICC1-4.

6.3.7 LED Current Control and Dimming

The maximum current for each LED driver is the same – 100 mA. It is set by the resistor value R3. The application is configured for analogue dimming. The maximum current

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through the LED stack is 400 mA (4 x 100 mA). It is achieved at full scale ADIM voltage of 1.5 V.

Other dimming options are available, such as PWM, Sequenced PWM and combinations of Analog and PWM. For details, please see latest data sheet for InnoMux on the Power Integrations website.

6.3.8 Output Power Limiting

A power limit is implemented individually for each output using the PLIM1 and PLIM2 pins (U1 pins 15 and 16). The power delivered to any of the main outputs is restricted by limiting the maximum average frequency at which an output can receive charge pulses. The frequency limit is set by a passive network connected to the PLIM pins. Namely, resistor R4 connected to pin PLIM1 sets the frequency limit for output CV1; capacitors C45 and C46 set the frequency limit for CV2; and R40 connected to pin PLIM2 sets the frequency limit for the LED output. If the frequency is exceeded for a predetermined time interval, the InnoMux controller will execute auto-restart.

6.3.9 Standby Mode

If the STDBY input is held at 0 V the PSU enters ”Standby Mode”. The LED current is disabled and the LED driver circuit is powered down, reducing the controller own power consumption. Full rated power is still available at the CV1 and the CV2 outputs. The +V_LED output is maintained at a level of at least 15 V. The STDBY input is a logic level type. If it is pulled up to above 3.3 V (5 Vmax), the LED current will be enabled.

6.3.10 Start-Up Sequence

Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 8
Pri Switch V_{DS} [V]	V_{CV1} [V]	V_{LED} [V]	V_{BP} [V]	U1/2 REQ pin [V]	U1/2 ACK pin	LED Output Current [A]

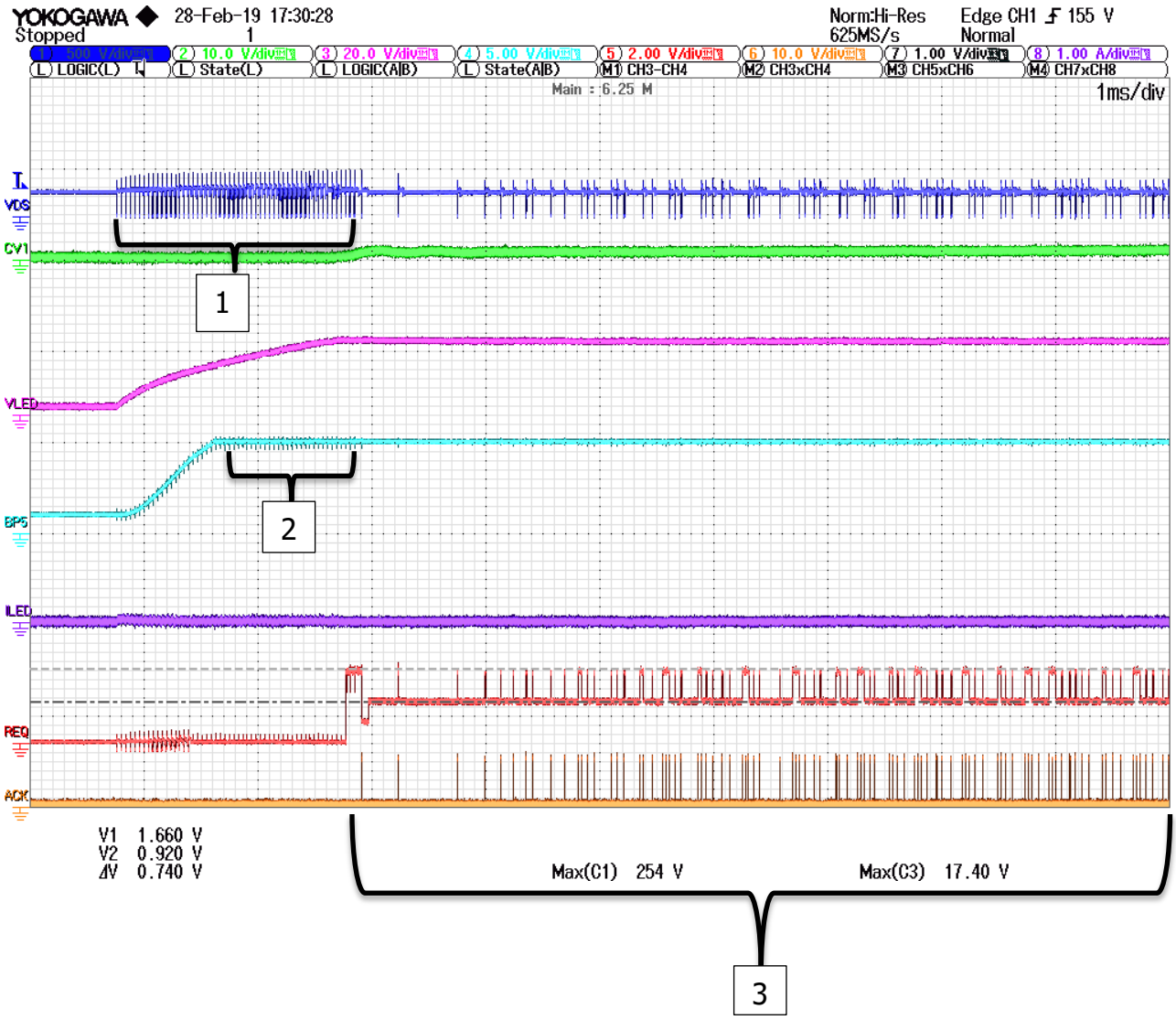

Figure 5 – First 10 ms of Start-Up.

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1. Secondary-side controllers are powered-down (asleep). The primary-side controller operates open-loop at a fixed frequency about 25 kHz. The peak current is set to approximately 75% of its maximum level. If the secondary-side does not wake up and respond, the primary-side will:
   a. time out and shut down, or
   b. the primary-side bias voltage will rise high enough to trigger a bias OVP shutdown.
2. The LED output is the only output to rise significantly during interval 1. It provides power to InnoMux (U1) internal voltage regulator (BP regulator), which generates the internal supply bus BP (+5 V). Note that the BP rail is common for both U1 and U2. Eventually the internal voltage regulator establishes 5 V at the BP pin. U1 and U2 secondary-side controllers then initialize. U1 sends a request signal to the secondary controller. (U1 pin 14 (REQ) is raised to ~1.7 V)
3. When the InnoSwitch3-MX (U2) secondary-side controller recognizes the request signal from U1, it sends a request pulse to the primary-side of U2 and an acknowledge pulse to U1 (ACK pin U2 pin 4). U1 recognizes the ACK signal and de-asserts the REQ signal - 'No Pulse Request' level (~0.9 V). IC U1 then sets the state of Q2 and Q4 to direct the requested flyback pulse to the appropriate output.
4. CV1, CV2, and LED output voltages can be seen to rise simultaneously (Figure 6). At some time during interval 4, the CV2 will reach a sufficient level to power the internal BP regulator via the VCV2 pin (U1 pin 25). The input of the BP regulator then switches automatically to the VCV2 pin, thus reducing the power dissipation in the BP regulator.

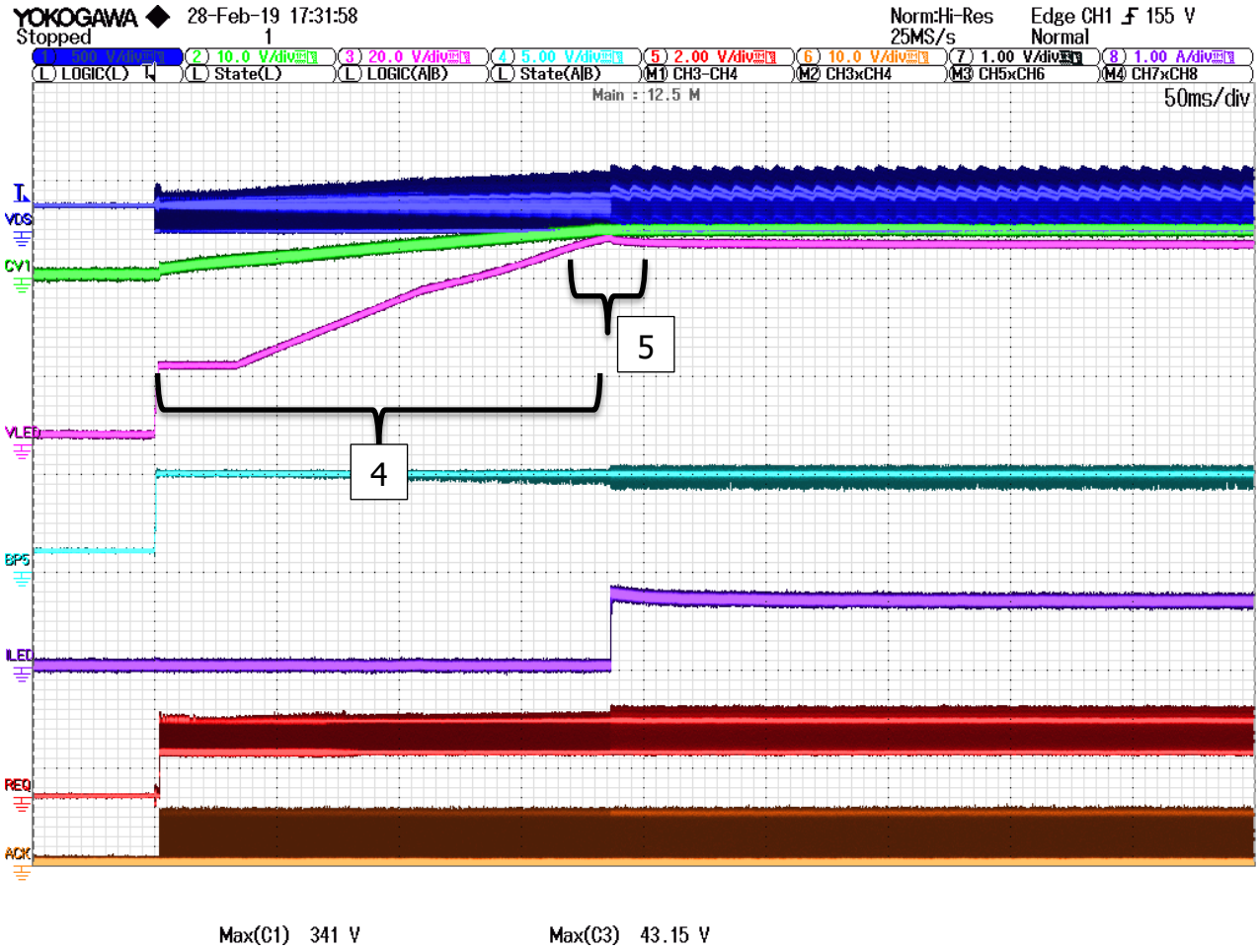

Figure 6 – Complete Start-Up Cycle Over Approximately 230 ms.

5. The LED current is enabled. Its level depends on the dimming configuration and the signal on the dimming input(s) (ADIM, PWM). The LED current is controlled by the internal LED drivers ICC1 to ICC4 (U1 pins 1, 2, 4 and 5), which in this case are connected in parallel. To reduce its own dissipation the InnoMux controller (U1) maintains V_{LED} at a level with some minimum headroom of above the LED stack voltage. This keeps the voltage at the ICC pins to a minimum.

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7 DER-871 Connection Diagram

The connection diagram on Figure 7 below shows an analogue dimming configuration. For other dimming configurations, please refer to the product datasheets.

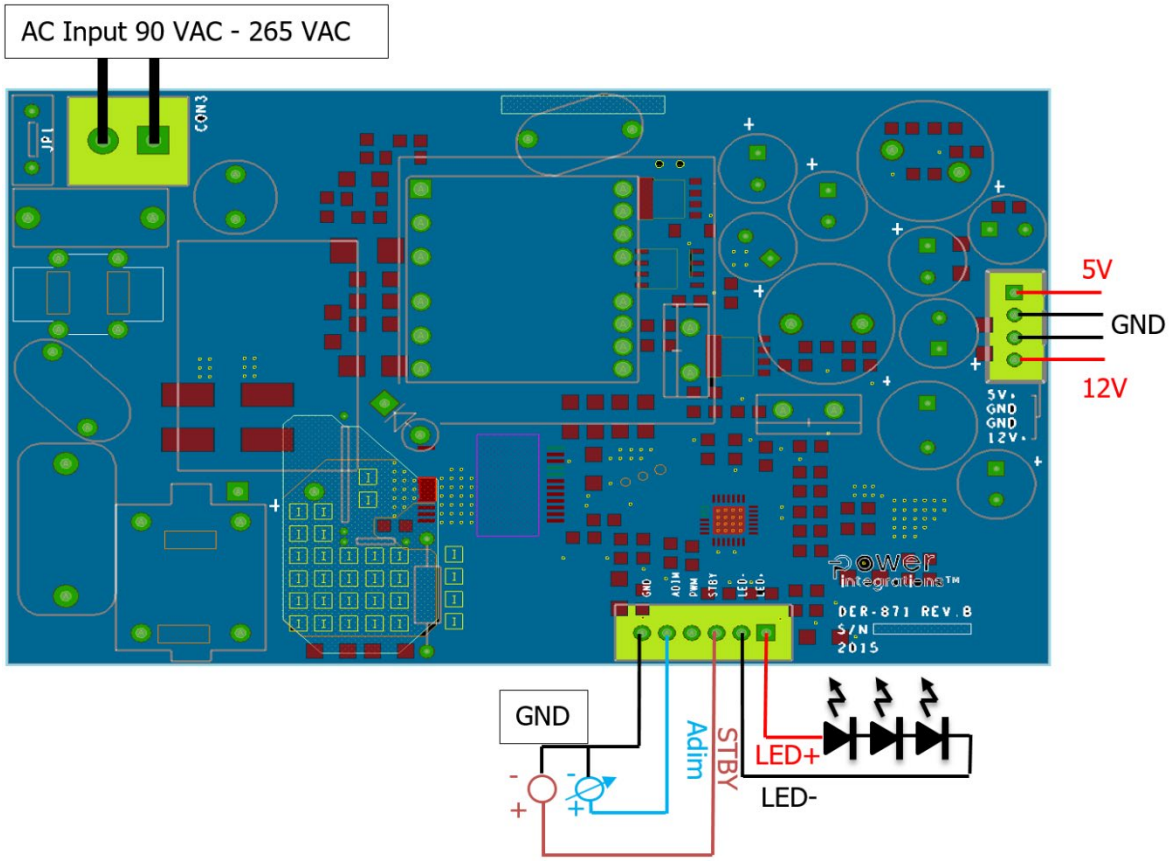

Figure 7 – Connection Diagram

8 PCB Layout

The converter PCB layout is illustrated on Figure 8, Figure 9 and Figure 10 below. PCB copper thickness is 2 oz (2.8 mils / 70 μm) was used for the PCB. To minimize crosstalk between the outputs of the converter, it is essential to minimize the length of the connection between the negative terminals of C10, C25, C13, C14 and C15 to the source of the SR MOSFET (Q1). The three AC current paths for all outputs to the source of Q1 should be kept separate.

Ideally, the connection between the GND pins of U1 and U2 should not be shared with any AC ripple current in the output filter stages. This is important for achieving accurate synchronous rectification.

The primary switch in InnoSwitch3-MX IC (U2) is cooled through the SOURCE pin (the paddle) of the IC. Care should be taken that the thermal impedance between the paddle and the cooling copper of the PCB is kept to a minimum. For best results the cooling copper pour should flair out as rapidly as possible away from the solder joint (Figure 8).

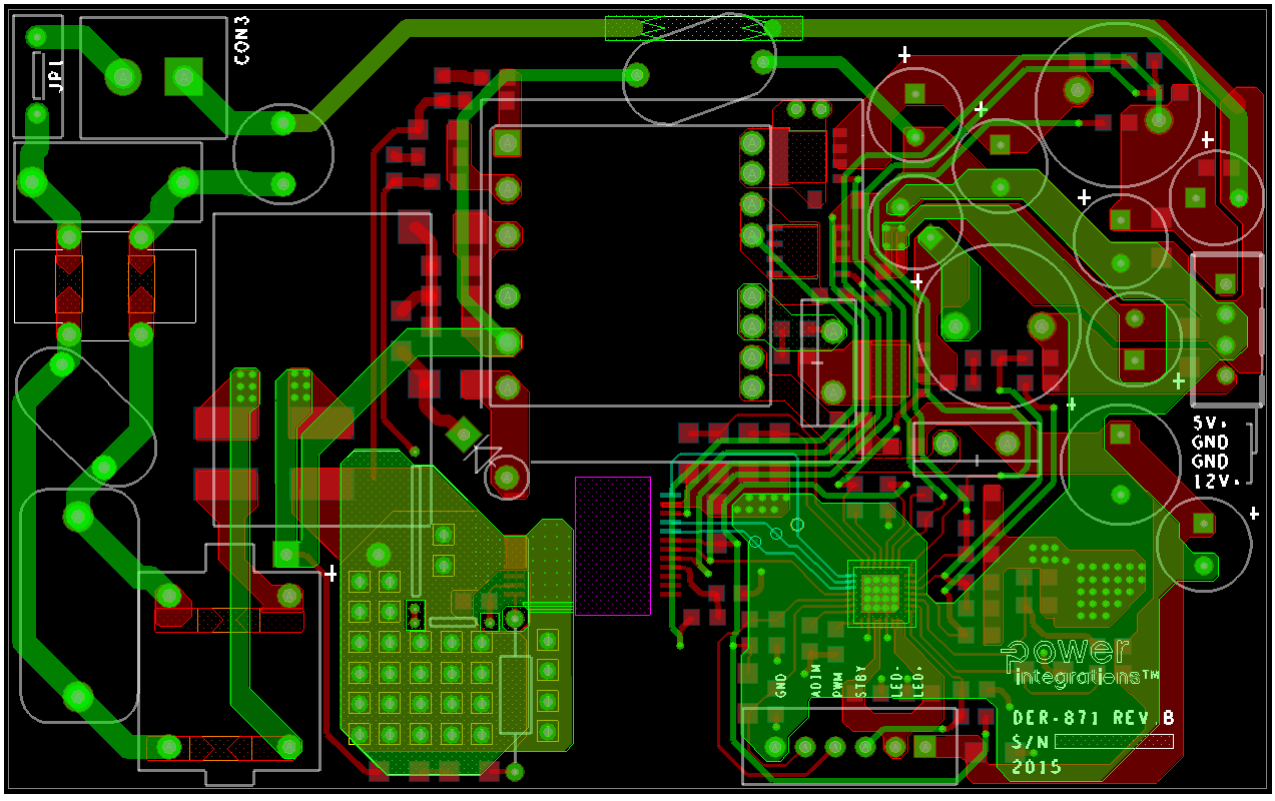

Figure 8 – Printed Circuit Layout.

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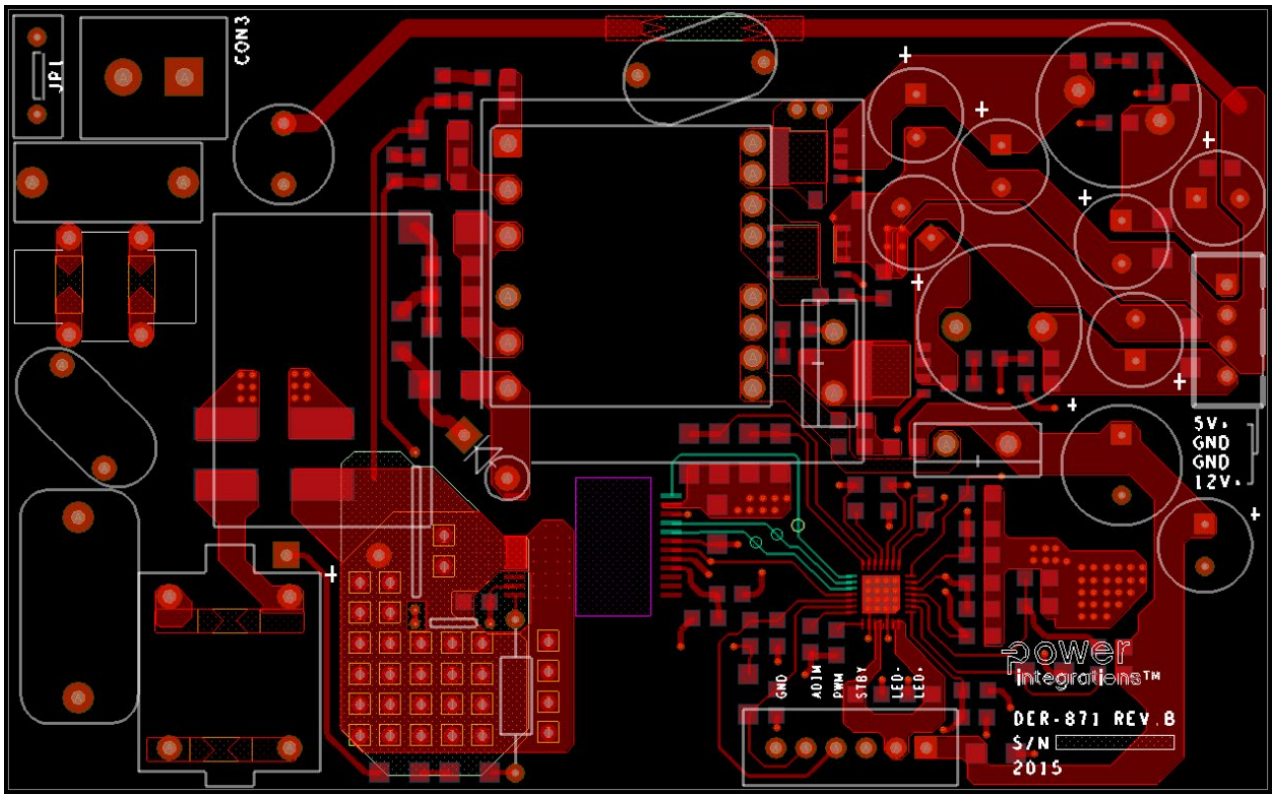


Figure 9 – Printed Circuit Layout, Bottom.

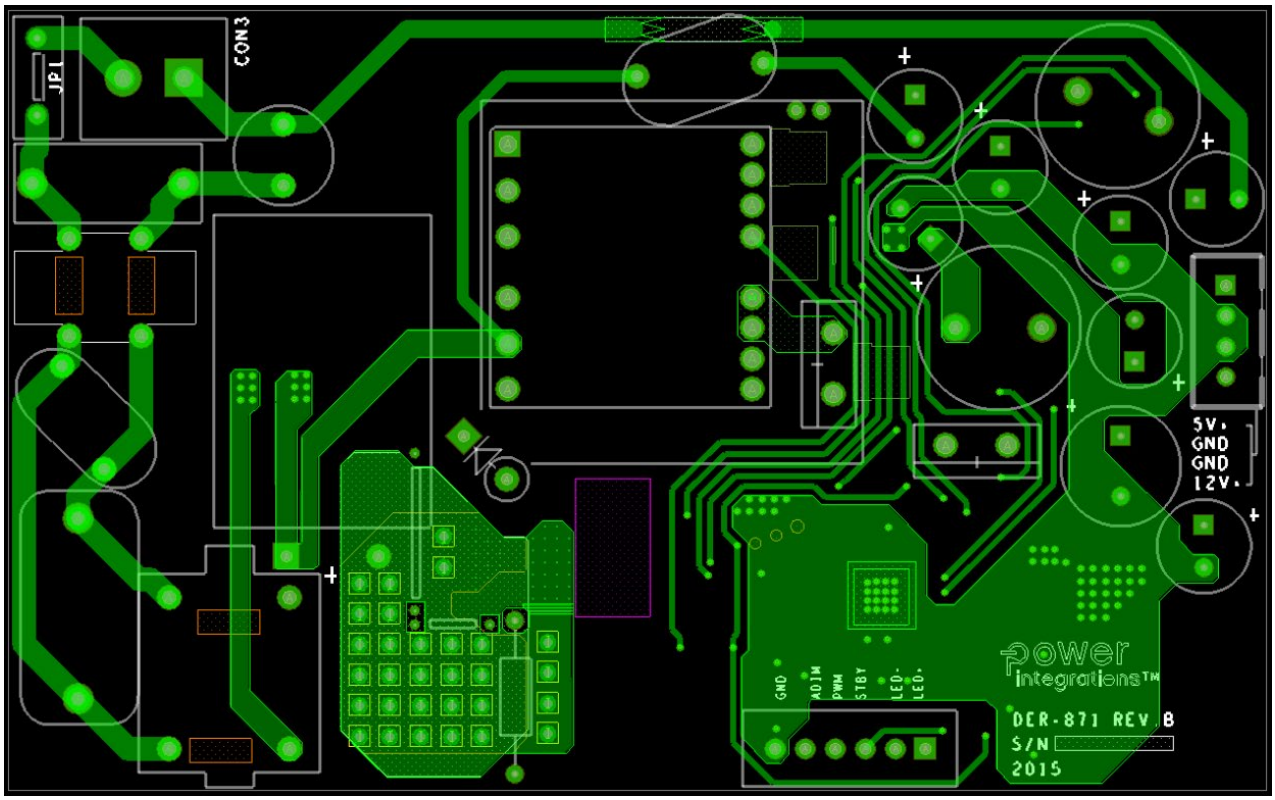
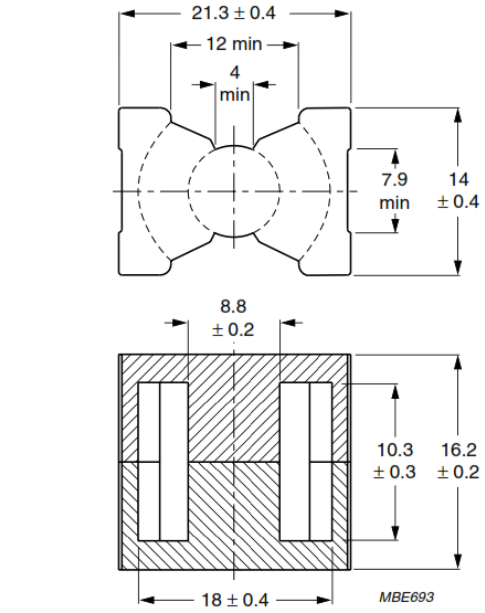


Figure 10 – Printed Circuit Layout, Top.

9 Transformer (T1) Specification

9.1 *Core Information*

Core PQ20/16, Ferroxcube Part No. PQ20/16-3C95



Dimensions in mm.

Fig.1 PQ20/16 core set.

Figure 11 – PQ20/16 Core – Geometry.

SYMBOL	PARAMETER	VALUE	UNIT
Σ(l/A)	core factor (C1)	0.607	mm^{-1}
V_e	effective volume	2330	mm^3
l_e	effective length	37.6	mm
A_e	effective area	61.9	mm^2
A_{min}	minimum area	59.1	mm^2
m	mass of set	≈ 13	g

Table 1 – Core Characteristics.

GRADE	A_L (nH)	μ_e	AIR GAP (μm)	TYPE NUMBER
3C95 des	4080 ±25%	≈ 1970	≈ 0	PQ20/16-3C95

Table 2 – Core Material Specification.

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9.2 *Bobbin Information*

General data 14-pins PQ20/16 coil former

PARAMETER	SPECIFICATION
Coil former material	thermoplastic polyester, glass-reinforced, flame retardant in accordance with *"UL 94V-0"*; UL file number E41938
Pin material	copper-tin alloy (CuSn), tin (Sn) plated
Maximum operating temperature	180 °C, *"IEC 60085"*, class H
Resistance to soldering heat	*"IEC 60068-2-20"*, Part 2, Test Tb, method 1B, 350 °C, 3.5 s
Solderability	*"IEC 60068-2-20"*, Part 2, Test Ta, method 1

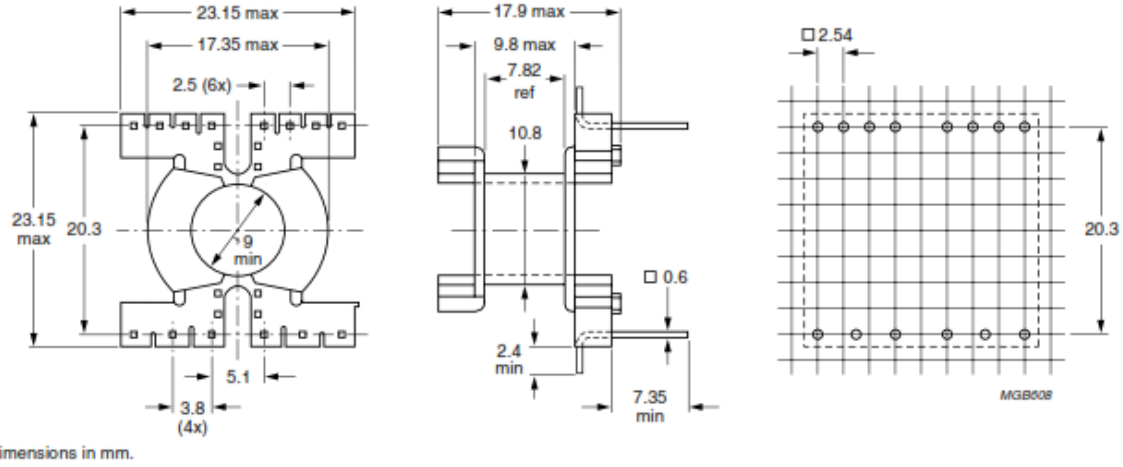

Fig.2 PQ20/16 coil former; 14-pins.

Winding data and area product for 14-pins PQ20/16 coil former

NUMBER OF SECTIONS	MINIMUM WINDING AREA (mm^2)	NOMINAL WINDING WIDTH (mm)	AVERAGE LENGTH OF TURN (mm)	AREA PRODUCT Ae x Aw (mm^4)	TYPE NUMBER
1	23.5	7.95	44.0	1450	CPV-PQ20/16-1S-14P
1	23.5	7.95	44.0	1450	CPV-PQ20/16-1S-14PD

Figure 12 – Ferroxcube PQ20/16 - 14 Pin Bobbin – CPV-PQ20/16-1S-14P.

9.3 *Electrical Diagram*

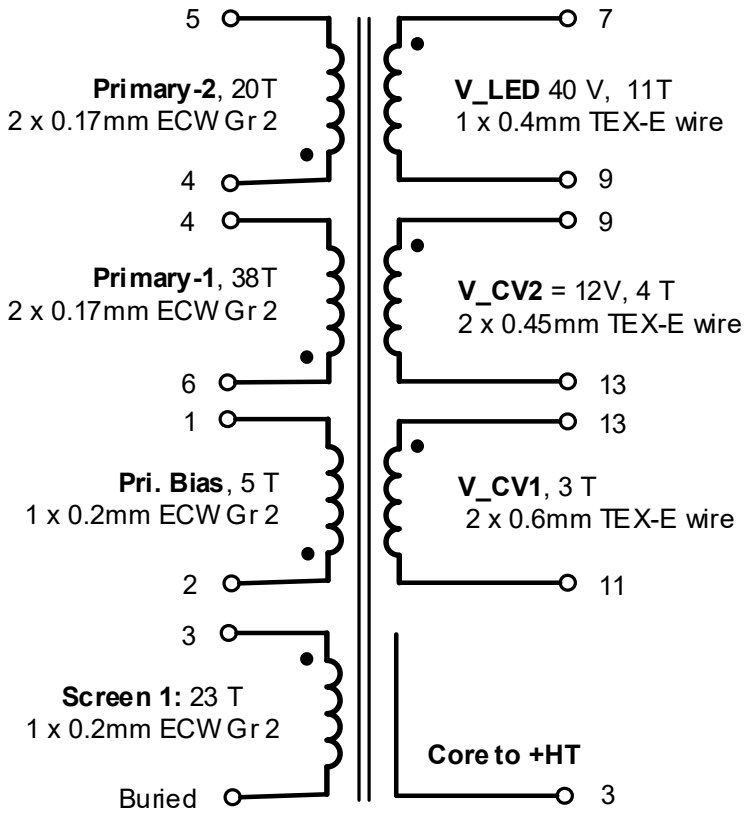

Figure 13 – Transformer Electrical Diagram.

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9.4 *Winding Stack Diagram*

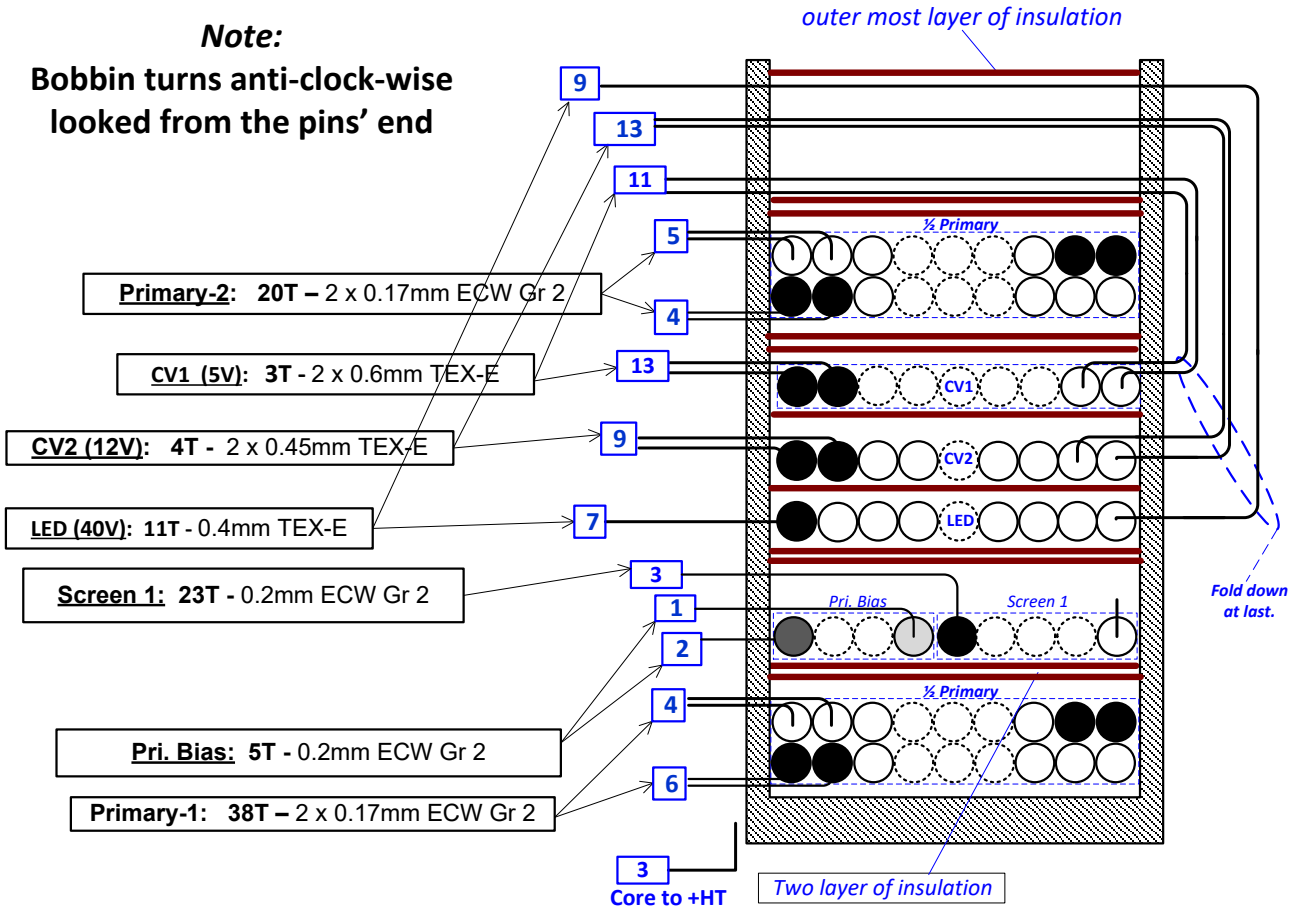

Figure 14 – Transformer Build Diagram.

9.5 *Transformer Electrical Specification*

Parameter	Condition	Spec.
Electrical strength	1 second, 60 Hz from pins 1-6 to 7-13.	3000 VAC
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 5 and 6, with all other windings open.	785 µH ±3%
Resonant Frequency	Between pin 5 and 6, other windings open.	1,100 kHz (Min.)
Primary Leakage Inductance	Between pin 5 and 6, with all secondary 7, 9, 11 and 13 shorte	6 µH (Max.)

9.7 *Materials List*

Item	Description	Quantities
[1]	Core: Ferroxcube Part No. PQ20/16-3C95.	2
[2]	Bobbin: CPV-PQ20/16-1S-14P.	1
[3]	Magnet Wire: 0.17 mm ECW Gr 2.	510 cm
[4]	Magnet Wire: 0.2 mm ECW Gr 2.	123 cm
[5]	Magnet Wire: 0.37 mm, Triple Insulated Wire.	44 cm
[6]	Magnet Wire: 0.45 mm, Triple Insulated Wire.	35.2 cm
[7]	Magnet Wire: 0.6 mm, Triple Insulated Wire.	26.4 cm
[8]	Barrier Tape: Polyester Film, 1 mil thickness, 10 mm Wide.	70 cm
[9]	Clamps: Ferroxcube CLM/P-PQ20/16.	2
[10]	Bus Wire: #30 AWG.	20cm
[11]	Varnish: MR8008B - Varnish, Insulating, Polyurethane, Transparent/Amber EMR8008B250ML Or BC-359	5 ml

9.8 *Transformer Construction*

Layer 1 Primary-1	Start at pin 6, wind 38 turns of 2 wires Item [3] in 2 layers with tight tension. Terminate at pin 4.
Insulation	Place 2 layers of tape Item [8] for insulation.
Layer 2 Primary Bias	Start at pin 2, wind 5 turns of wire Item [4] in 1/5 layer with tight tension and terminate at pin 1.
Layer 2 Screen: 1	Start at pin 3, take wire Item [4] to end of bias wind and secure with tape Item [8]. Wind 23T to fill the rest of the bobbin width.
Insulation	Place 2 layers of tape Item [8] for insulation. Cut end of screen wind to leave the end buried under the tape.
Layer 3 LED	Start at pin 7, wind 10 turns of wire Item [5] in 1 layer with tight tension, at the last turn leave ~4 cm of wire for the termination.
Insulation	Place 1 layer of tape Item [8] for insulation.
Layer 4 CV2	Start at pin 9, wind 4 turns of 2 wires Item [6] in 1 layer with tight tension, at the last turn leave ~4 cm of wire for the termination.
Insulation	Place 1 layer of tape Item [8] for insulation.
Layer 5 CV1	Start at pin 13, wind 3 turns of 2 wires Item [7] in 1 layer with tight tension, at the last turn leave ~4 cm of wire for the termination.
Insulation	Place 2 layers of tape Item [8] for insulation.
Layer 6 Primary-2	Start at pin 4, wind 20 turns of 2 wires Item [3] in 2 layers with tight tension. Terminate at pin 5.
Insulation	Place 2 layers of tape Item [8] for insulation.
CV1 Termination	Terminate CV1 wires to pin 11.
CV2	Terminate CV2 wires to pin 13.
LED	Terminate LED wire to pin 9.
Insulation	Place 1 layer of tape [8] for insulation and to hold secondary end wires in place.
Finish Assembly	Gap core halves to 785 µH ±3% inductance. Insert cores and tape tightly together item [8]. Solder TCW item [10] to pin 3, take across to core, wrap 2 turns vertically and solder to start. Cover with 1 layer of tape item [8]. Label "DER871 XXX.X µH" (XXX.X = measured primary inductance value in µH) Varnish - Item[11].

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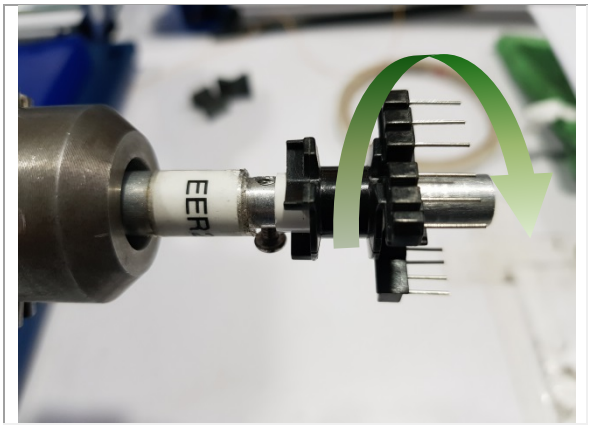
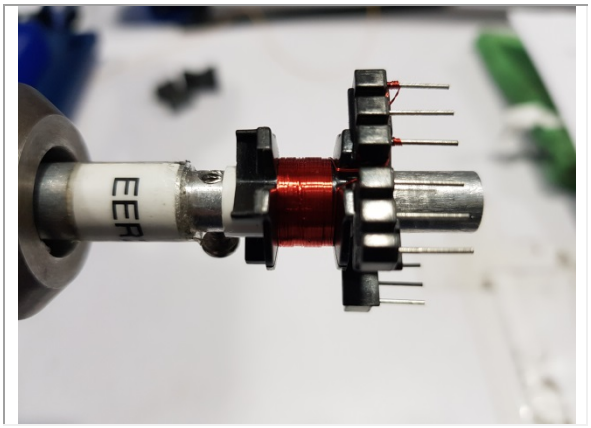
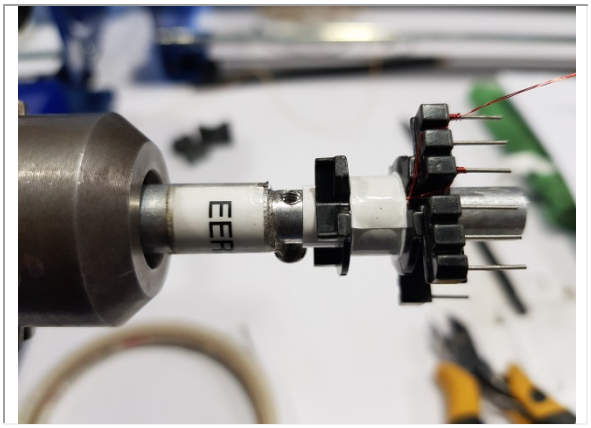
9.9 *Transformer Test*

The winding measured inductance of the individual windings as well as the primary leakage inductance of the transformer are shown in the table below:

		Between Pins	**Pins Shorted**
Lpri [μH]	784.7	5 - 6	
LCV1 [μH]	2.25	11 - 13	
LCV2 [μH]	11.8	11 - 9	
LLED [μH]	76.24	11 - 7	
L1Saux [μH]	6.5	1 - 2	
Llkg1 [μH]	25.9	5 - 6	7 and 9
Llkg2 [μH]	17.1	5 - 6	7 and11
Llkg3 [μH]	10.65	5 - 6	7 and 13

Table 3 – Winding Inductance. All measurement done in 100 kHz at 1 V_{RMS}.

9.10 *Winding Illustration*

		Place the bobbin on the mandrel with the pin side to the right. Winding direction is in the clockwise direction i.e. top side moving away from operator.
Wind 1 **Primary 1** **½ Primary**		Start at pin 6, bring wires across through slot between pins 5 & 6. Close wind 38 turns, 2 strands of wire Item [3] in 2 layers with tight tension to fill the bobbin width in a neat flat wind.
Insulation layer		Use 2 turns of tape, Item [8], to cover the winding. Take the wires through slot between pins 3 and 4 and finish at pin 4.

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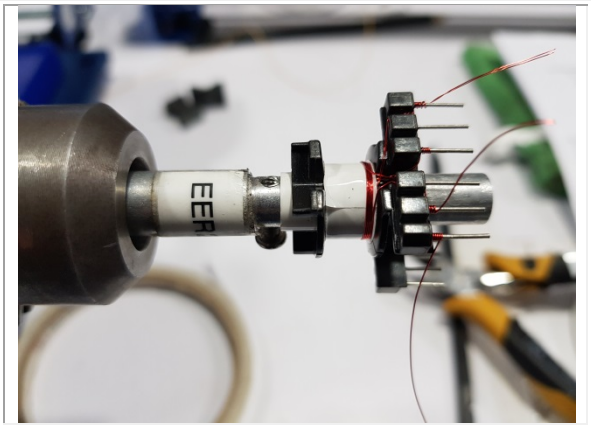
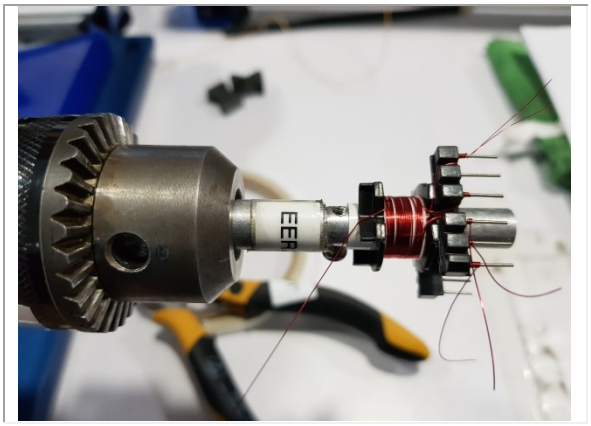
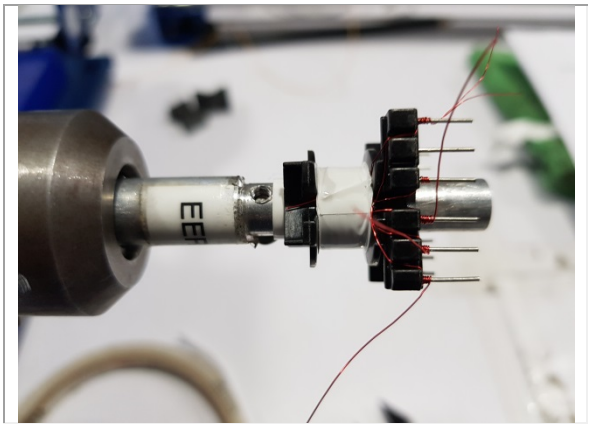
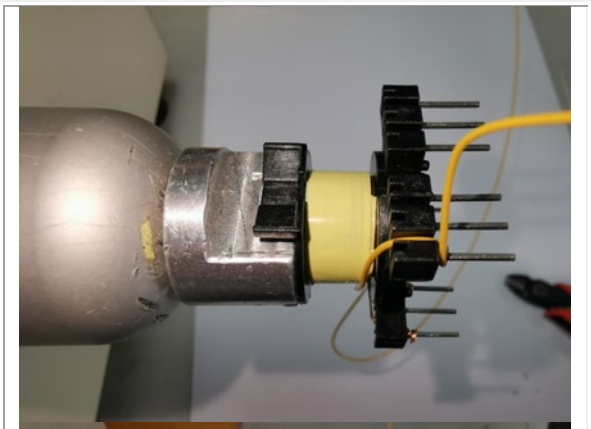
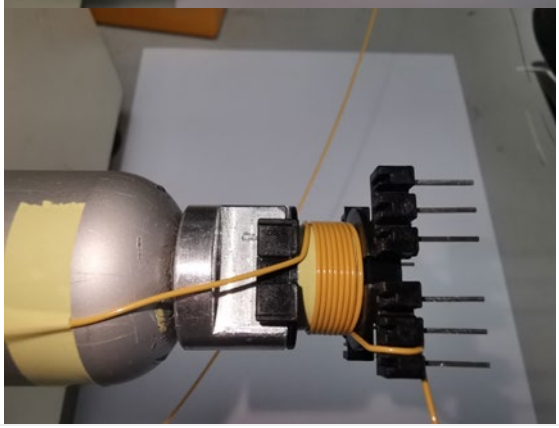
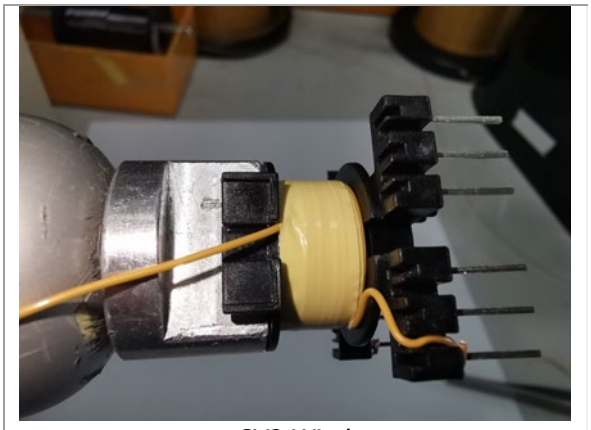
Wind 2 **Primary Bias**		Start at pin 2, bring wire across through slot between pins 1 & 2. Close wind 5 turns, 1 strand of wire Item [4] in 1/5th layer with tight tension. Take the wire through slot between pins 1 & 2 and finish on pin 1.
Wind 3 **Screen 1**		Start at pin 3, bring wire through slot between pins 2 & 3. Place 1st turn at the end of the Primar Bias winding. Close wind 23 turns 1 strand of wire item [4] with tight tension to fill the remaining bobbin width.
Insulation layer		Hold winding in place with ½ turn of tape item [8] and cut wire off to form a buried free end. Add tape to make up to 2 turns.

Wind 4 **LED**	 	Start at pin 7, bring wire across through slot between pins 7 & 8. Close wind 11 turns, single strand Item [5] with tight tension. Cut to leave 5cm of free wire and secure it to the mandrel chuck with tape
Insulation	 CV2 Wind	Secure wind in place with 1 turn of tape Item [8].

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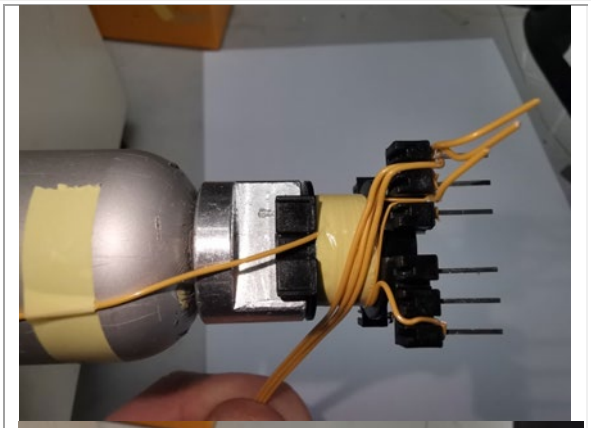
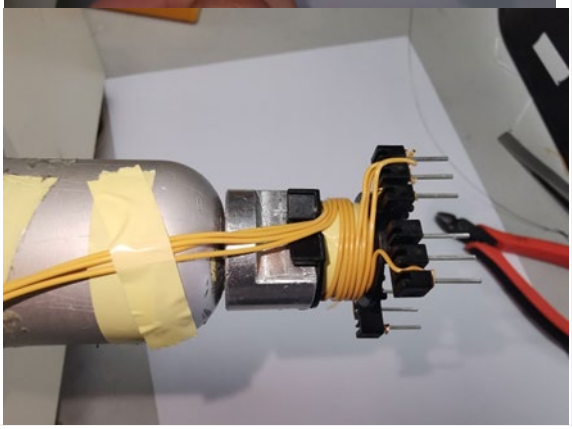
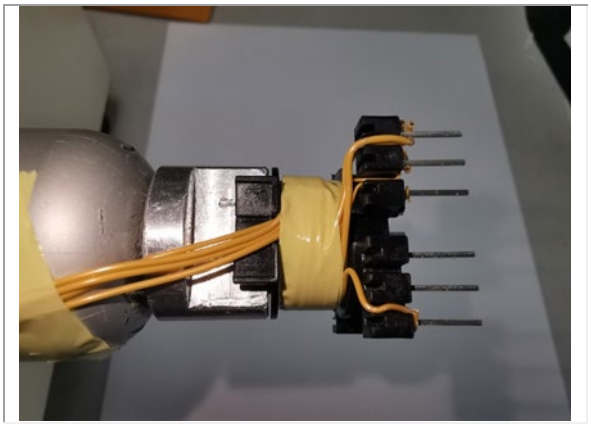
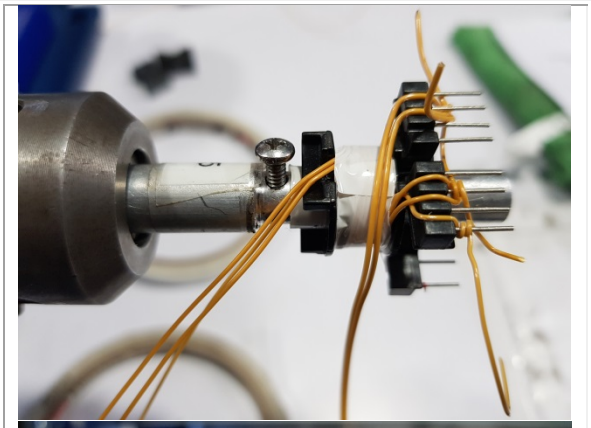
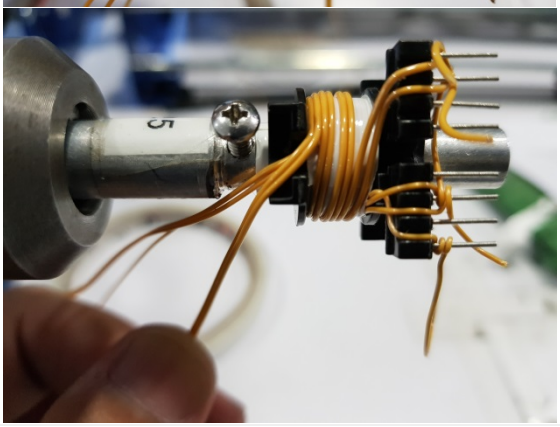
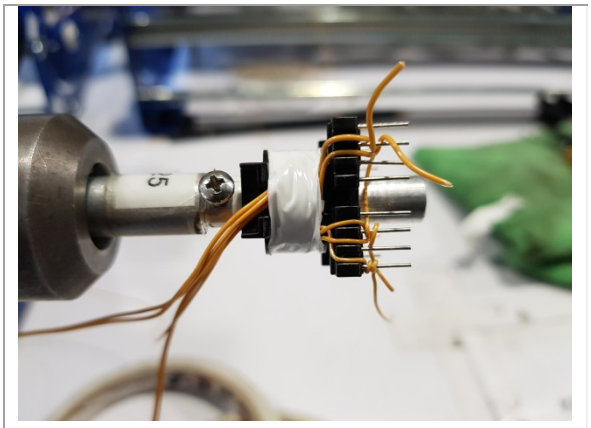
Wind 5 **CV2**	 	Start at pin 9 with 2 strands item [6], bring up through the slot between pins 9 & 10. Wind 4 turns tight wound to fill bobbin width. Cut to leave about 5cm and tape to mandrel bobbin.
Insulation		Secure wind in place with 1 turn of tape Item [8].

Wind 6 **CV1**	 	Start at pin 13 with 2 strands item [7], bring up through the slot between pins 12 & 13. Wind 2 turns tight wound to fill bobbin width. Cut to leave 5cm of free wire and secure it to the mandrel chuck with tape
Insulation		Secure wind in place with 2 turns of tape Item [8].

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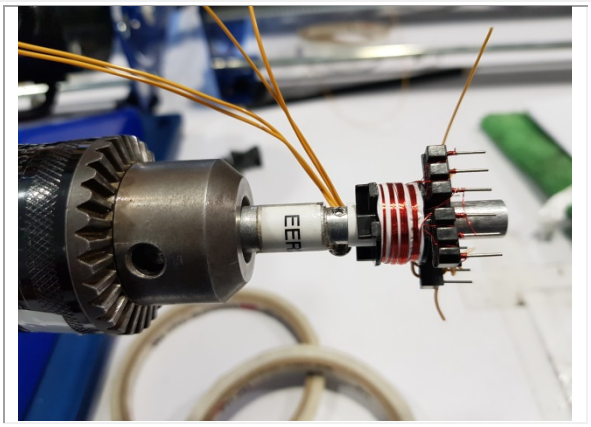
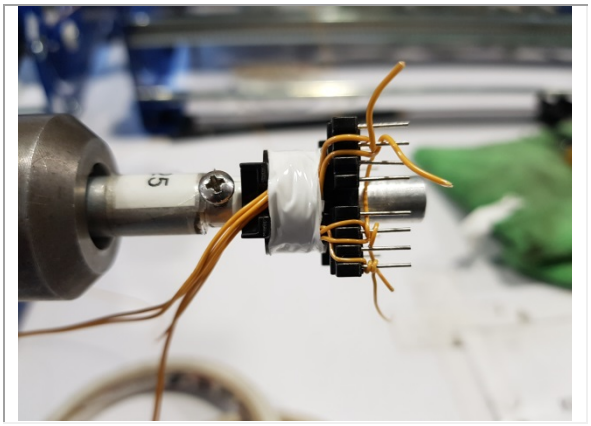
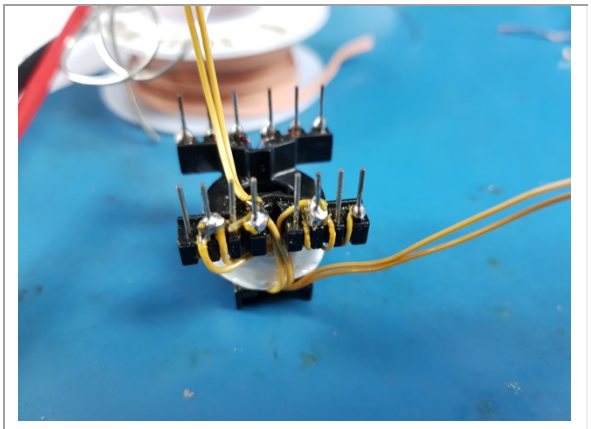
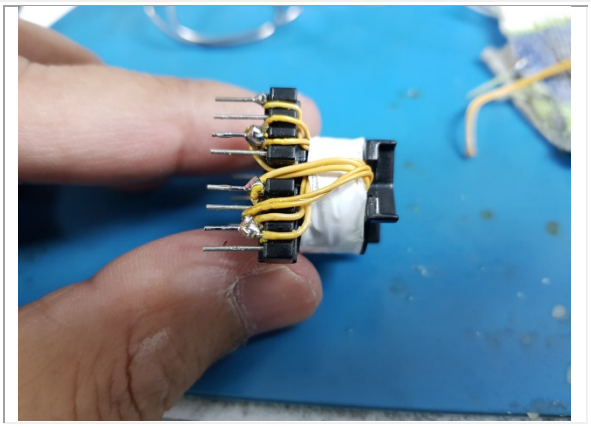
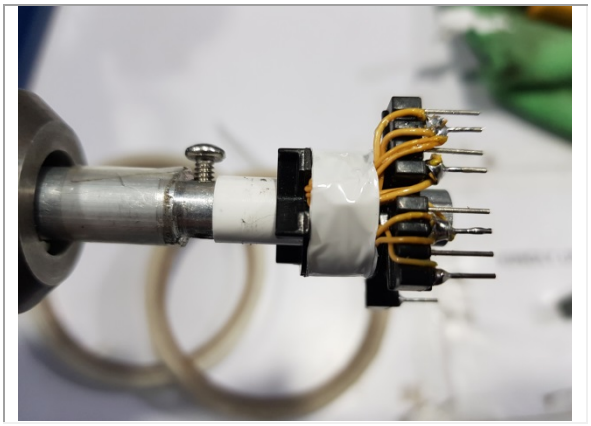
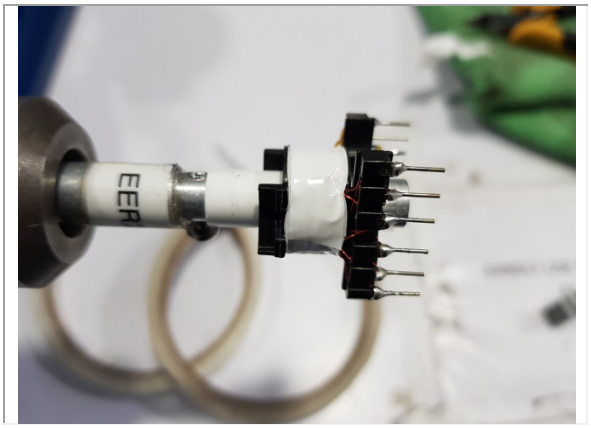
Wind 7 Primary 2 ½ Primary winding		Start at pin 4, bring wires across through slot between pins 3 & 4. Close wind 20 turns, 2 strands of wire Item [3] in 2 layers with tight tension to fill the bobbin width in as neat a flat wind as possible. Bring the wires down through the slot between pins 4 & 5. Terminate on pin 5.
Insulation		Secure wind in place with 2 turns of tape Item [8].
Terminate secondary winding ends		Bend LED wire end down and take through the slot between pins 9 & 10 and terminate to pin 9. Bend CV2 wire ends down and take through the slot between pins 13 & 14 and terminate to pin 13.

		Bend CV1 wire ends down and take through the slot between pins 10 & 11 and terminate to pin 11.
Insulation		Secure wind ends in place with 1 turns of tape Item [8].
		

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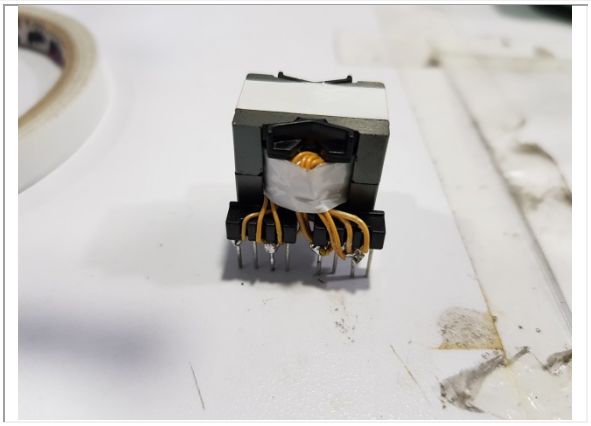
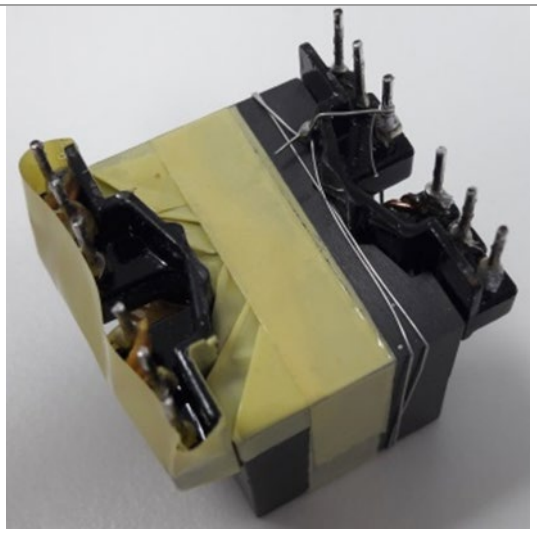
Insert bobbin		Gap core to achieve 785µH. Insert in bobbin. Tape core tightly together.
Core ground		Solder TCW item [10] to pin 3, take across to core, wrap 2 turns verticaly and solder to start.
		Cover with 1 layer of tape item [8]. Varnish dip and cure item [11]

10 Performance

10.1 *Full Load Efficiency vs. Line*

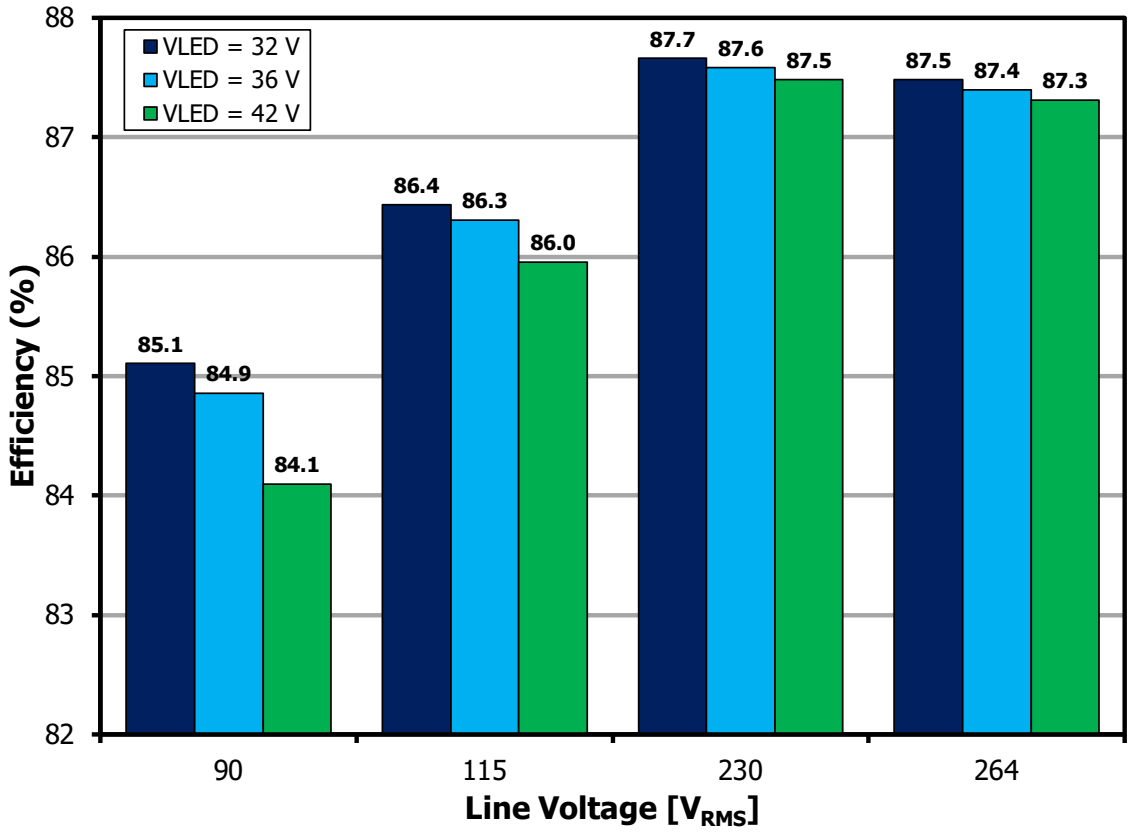


Figure 15 – Full Power Efficiency vs. Line Voltage at Room Temperature for Three Values of the LED Stack Voltage.

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10.2 *Efficiency vs. Load*

The efficiency vs. load measurements are shown below. These were obtained for all combinations of:

- All (nominal) UM line voltages;
- minimum, nominal and maximum LED stack voltage;
- LED total current of 30 mA, 230 mA and 420 mA;
- CV1 output current 0, 0.5 A and 1 A (0, 50% and 100% of FS);
- CV2 output current 0, 210 mA and 420 mA (0, 50% and 100% of FS)

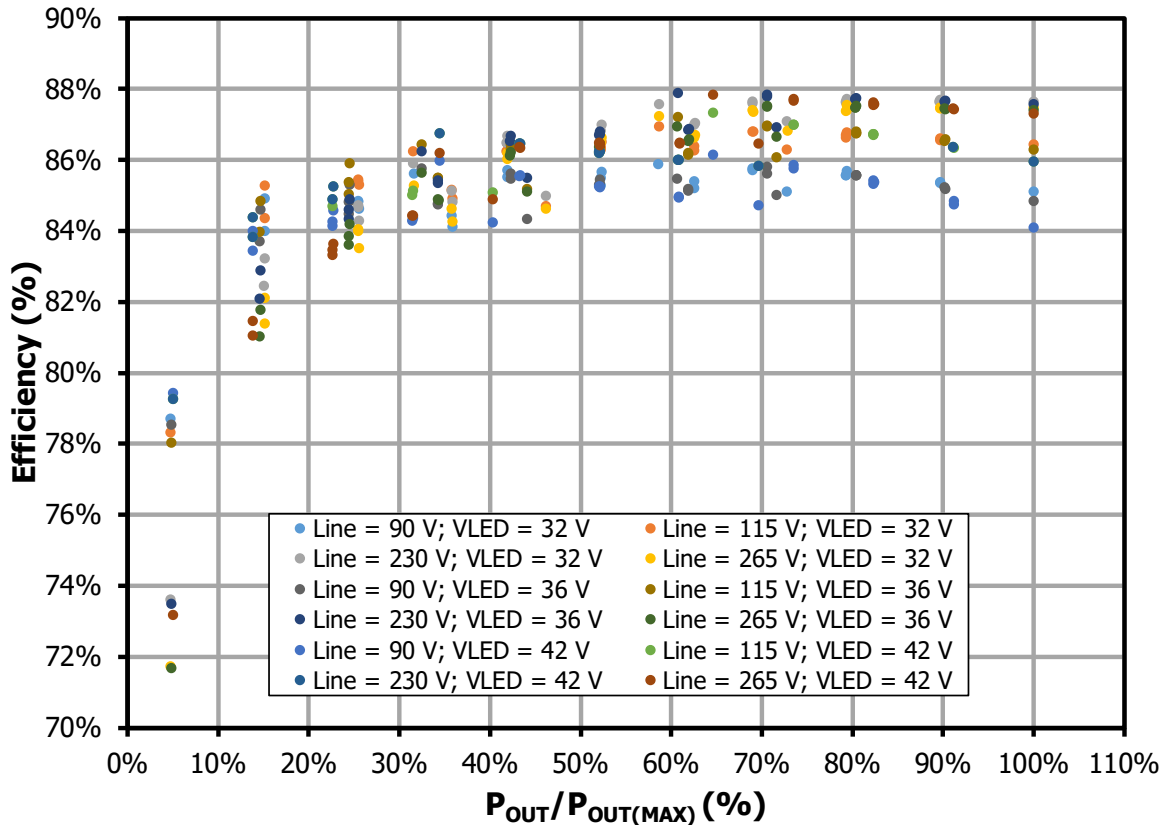

Figure 16 – Efficiency vs. Load for all line and V_{LED} variations, Room Temperature.

10.3 *Line Regulation at Full Load*

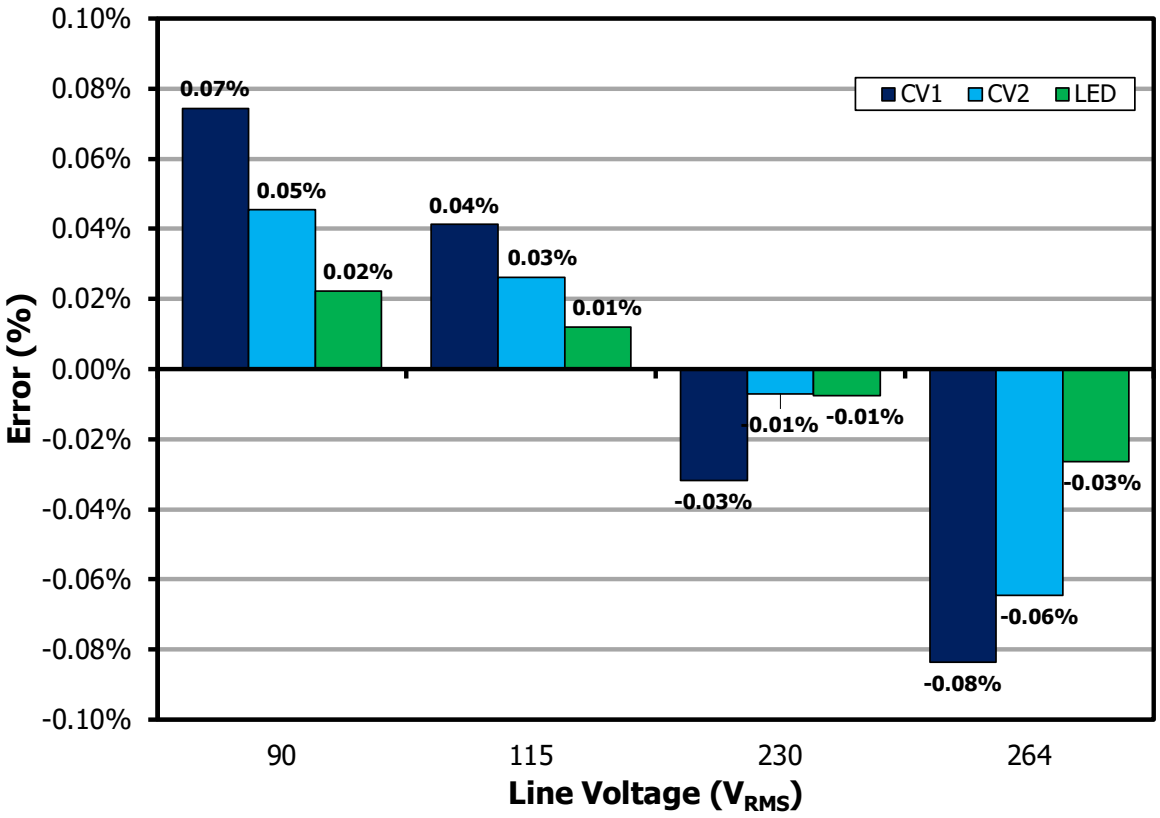

Figure 17 – Output Voltage Error vs. Line, Room Temperature.

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10.4 *Output Load Regulation*

The output-voltage regulation error was measured for both CV1 and CV2 output. The current at each output was increased from 1% to 100% of its rating in 5 steps. Measurements were taken for nominal LED stack voltage for all combinations of:

- all (nominal) UM line voltages
- 0% and 100% the LED rated output current

The load regulation error for the two CV outputs is shown on Figure 18 and Figure 19 below:

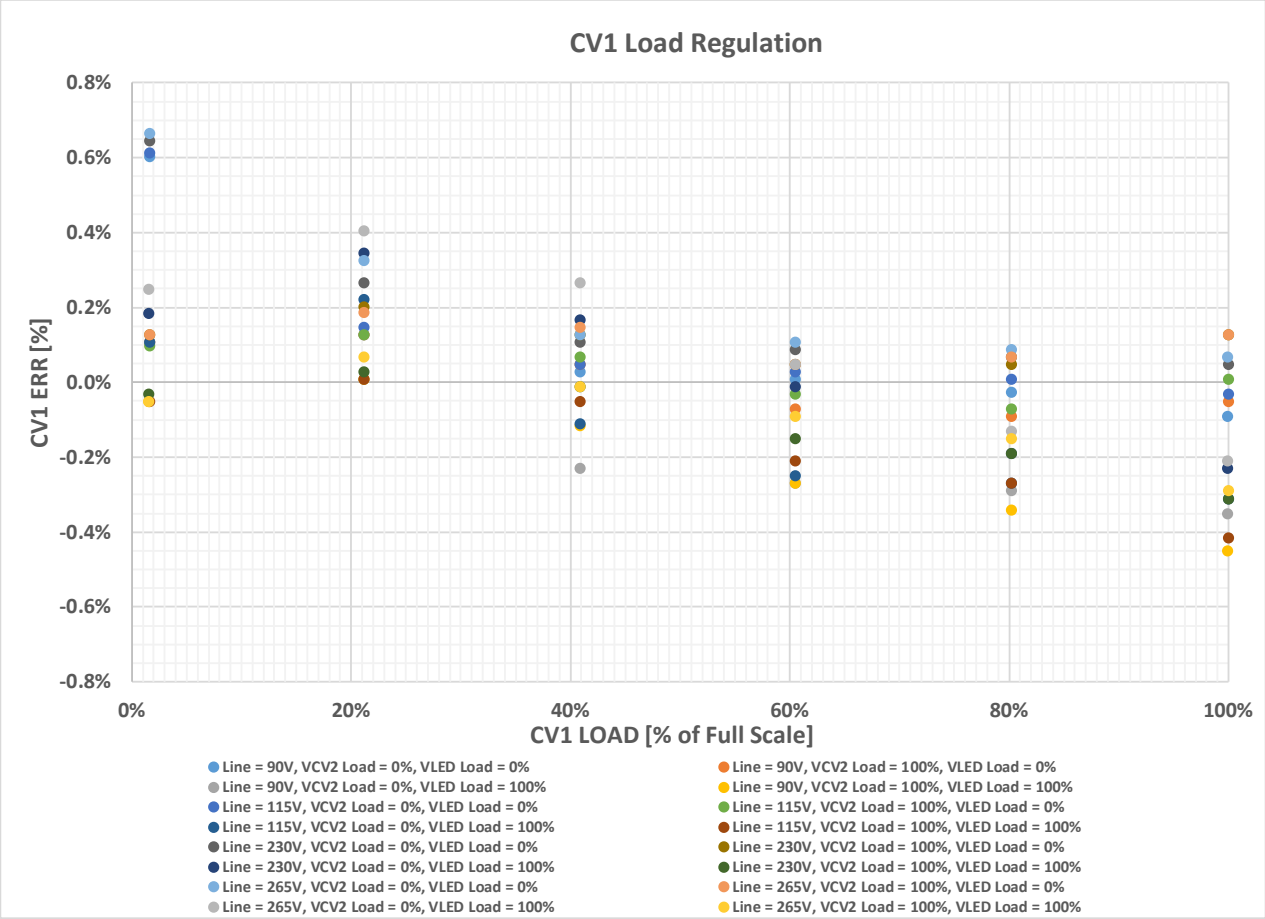

Figure 18 – VCV1 Output Error vs. Percentage Load, at Room Temperature.

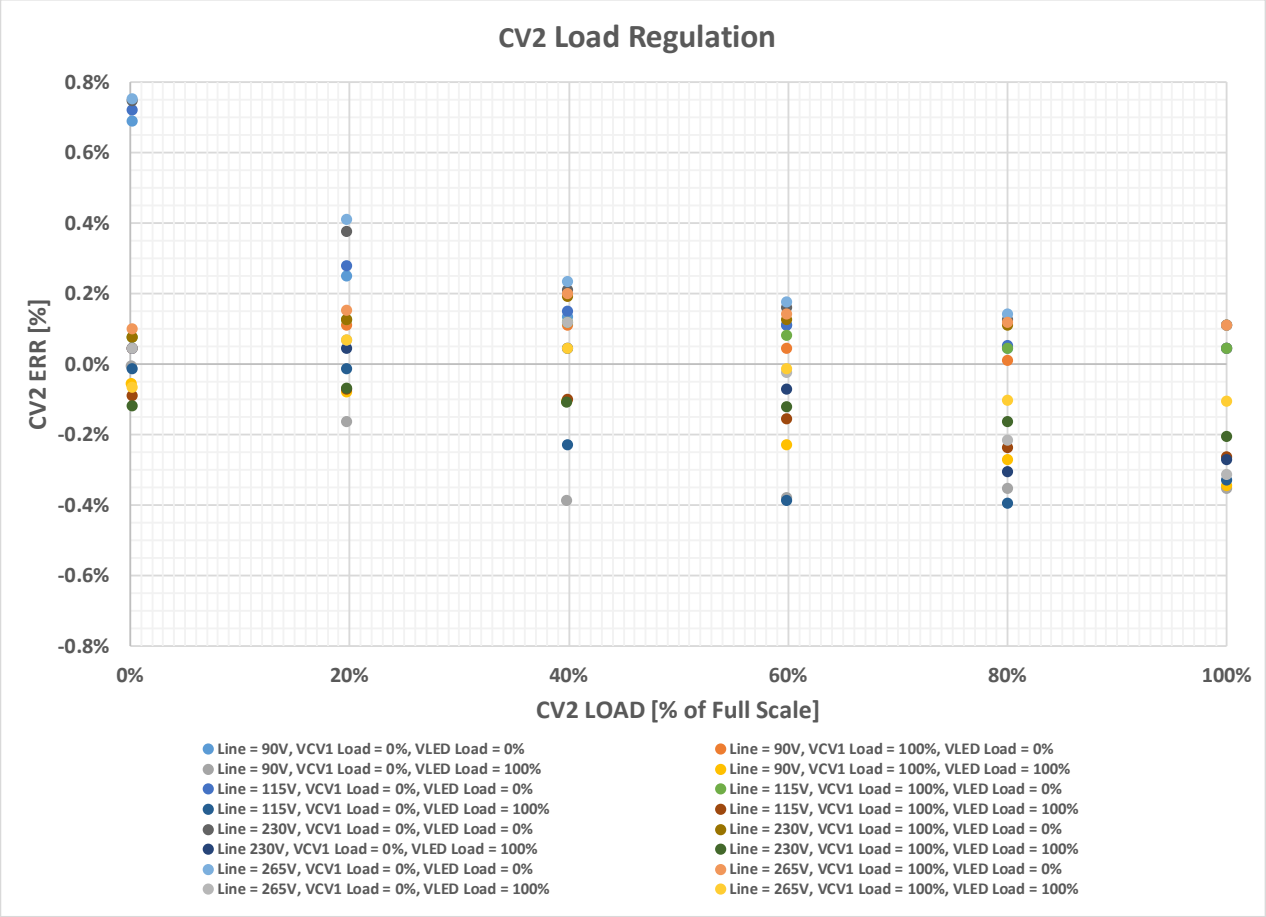

Figure 19 – VCV2 Output Error vs. Percentage Load, at Room Temperature.

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10.5 *Standby Input Power (I_{LED} = 0 A)*

The converter standby power was measured for all (nominal) line voltages; with no-load on the CV2 output; with the LED output current disabled for 0 mA, 10 mA and 20 mA load current on the CV1 (5 V) output. The results are shown in Figure 20 below.

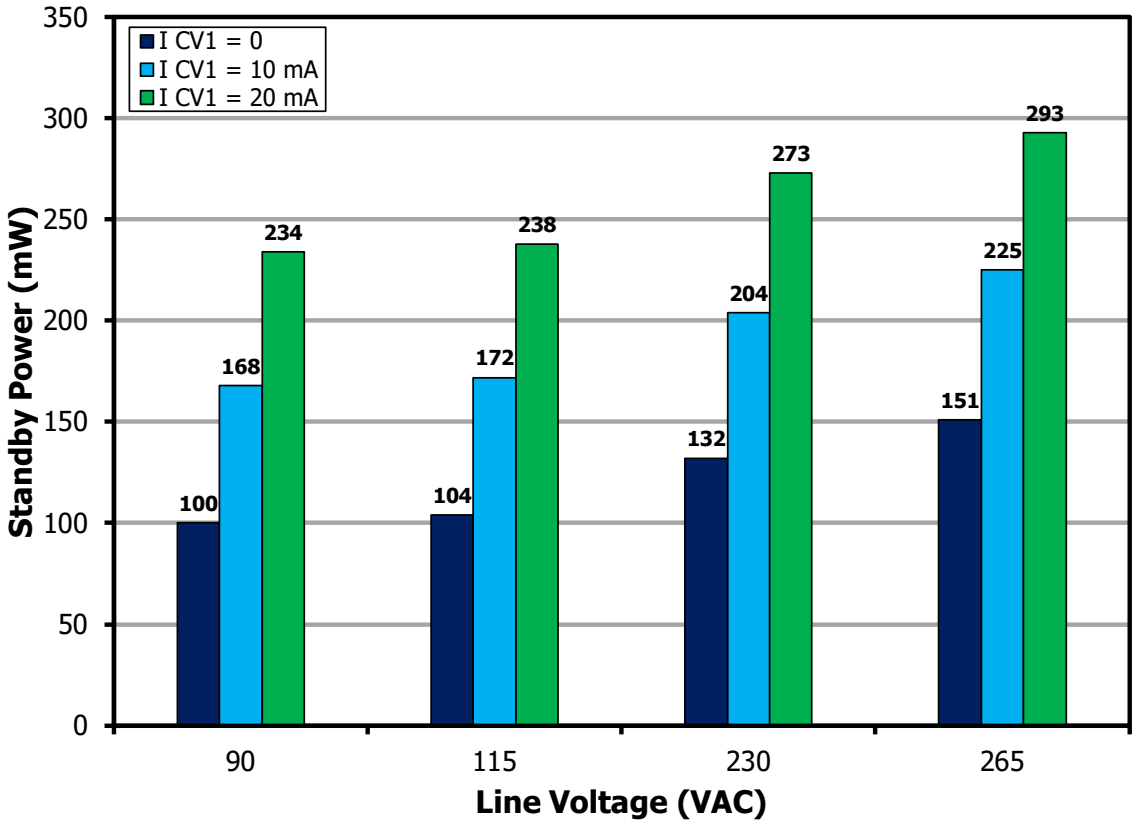

Figure 20 – Standby Power Consumption vs. Line Voltage, Room Temperature.

10.6 *LED Dimming*

The PSU was configured for analog dimming with FS ADIM input of 1.5 V. The value of the LED current was measured as the ADIM input voltage was increased from zero to FS in 10 steps. The measurements were taken at nominal LED stack voltage (36 V) and repeated for:

- all (nominal) line voltages;
- no load or full load on CV1 output;
- no load or full load on the CV1 output

The results are presented in Figure 21.

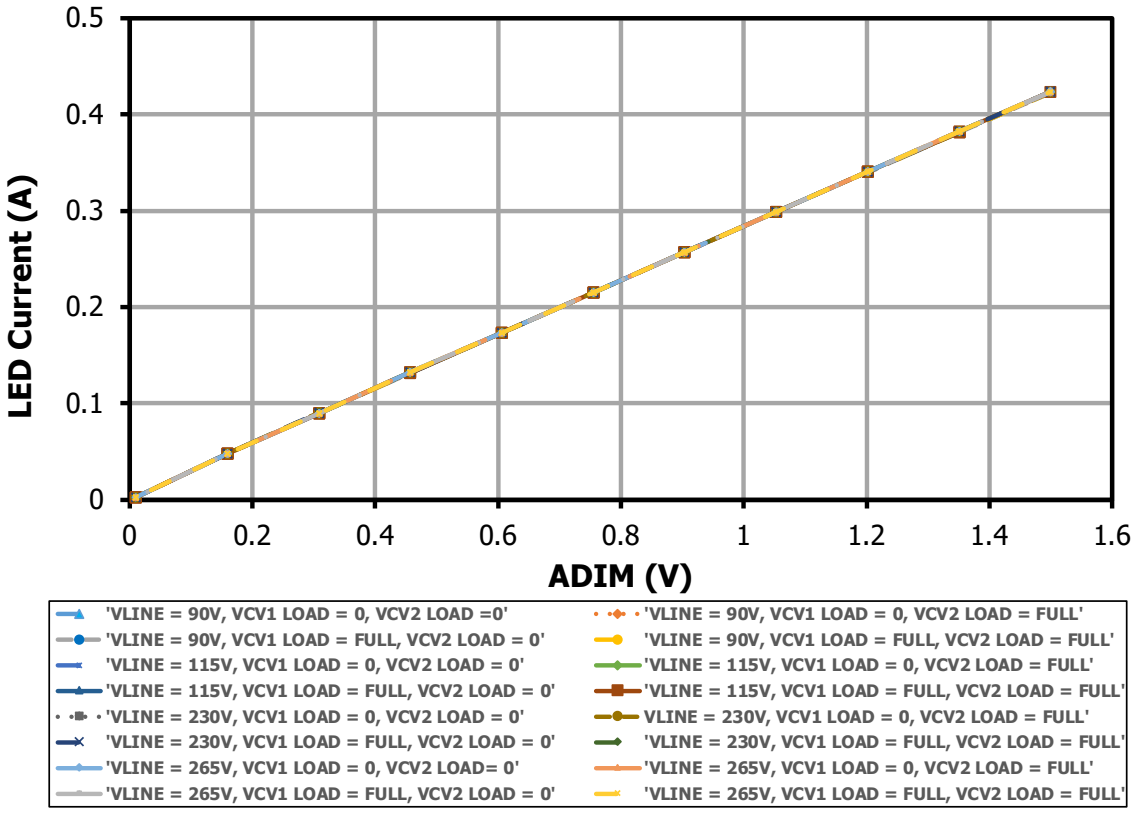

Figure 21 – Analog Dimming.

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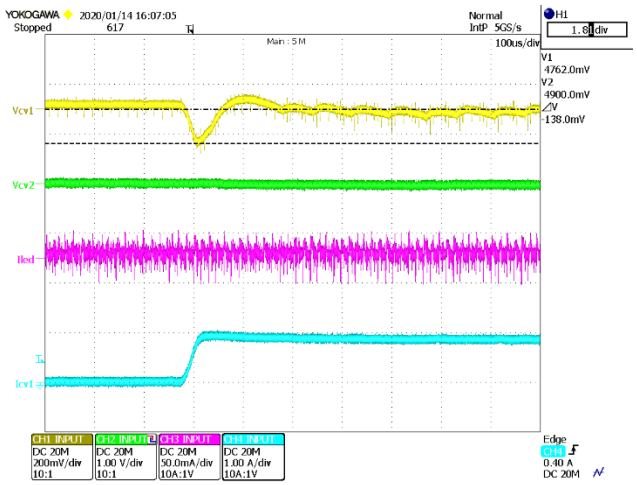
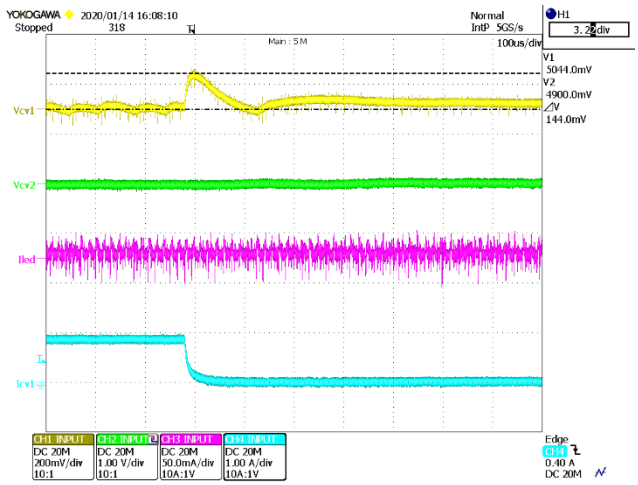
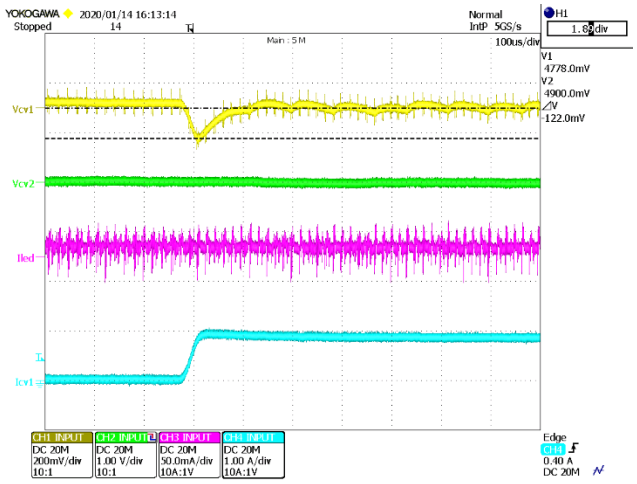
10.7 *Load Transient Response*

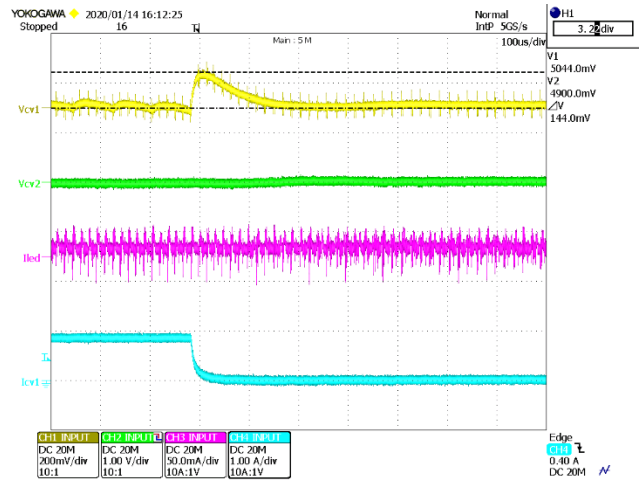
10.7.1 CV1 Step Load Transient





265 VAC, ICV1 = 0% -> 100%; ICV2 = 100%; ILED = 100%

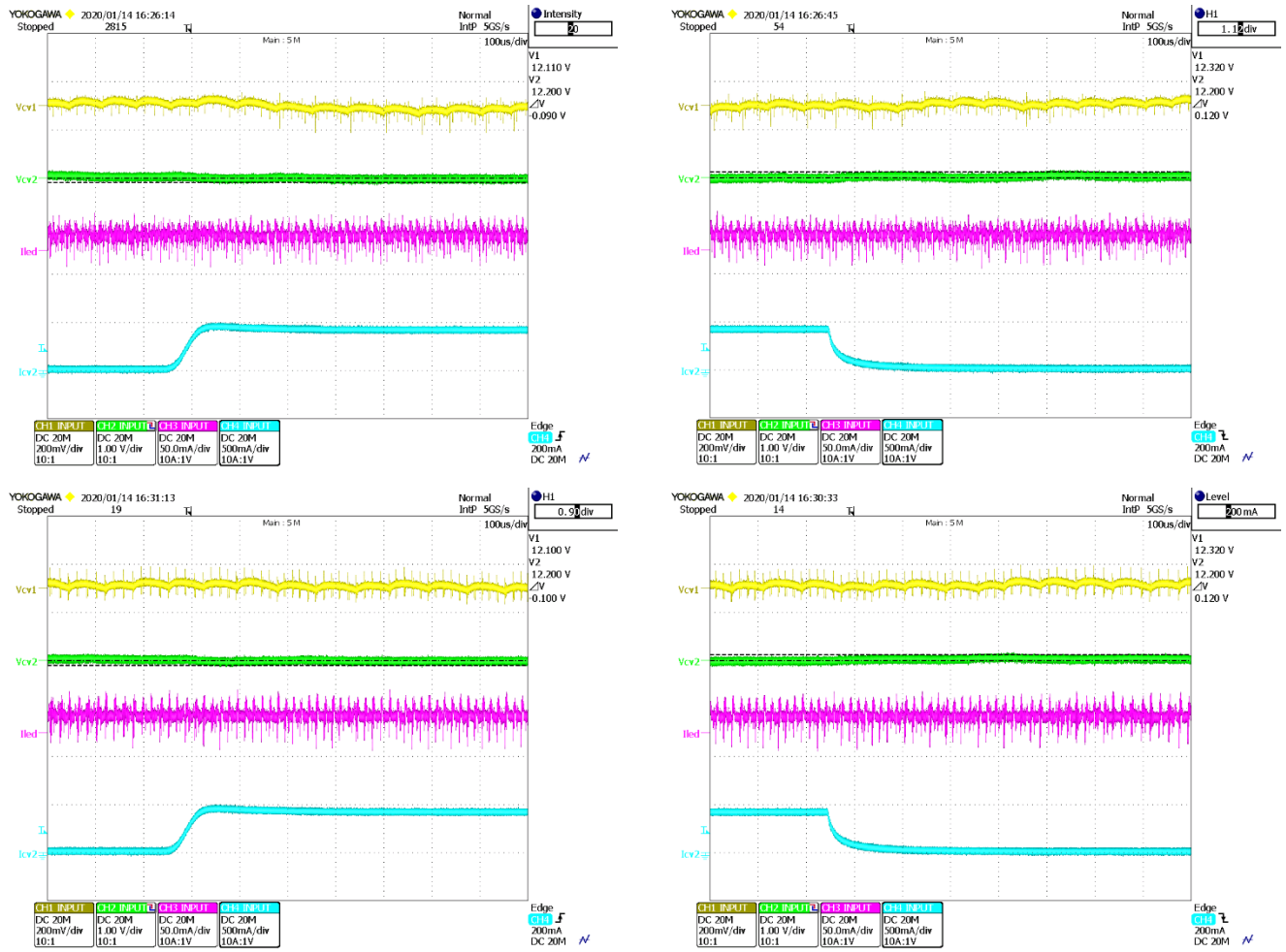




265 VAC, ICV1 = 100% -> 0%; ICV2 = 100%; ILED = 100%

Figure 22 – CV1 (5 V) Output - Load Transient (Overshoot 144 mV; Undershoot 138 mV).

10.7.2 CV2 Step Load Transient



265 VAC, ICV1 = 100%; ICV2 = 0% -> 100%; ILED = 100%

265 VAC, ICV1 = 100%; ICV2 = 100%-> 0%; ILED = 100%

Figure 23 – CV2 (12 V) Output - Load Transient (Overshoot 120 mV; Undershoot 100 mV).

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10.8 *Switching Waveforms*

10.8.1 Primary Switch Maximum Voltage

Voltages on the primary transistor drain to source on each pulse (LED, Vo2 and Vo1). Test condition is full load and maximum voltage, 375 VDC (equal to the peak of 265 VAC). A screenshot showing the worst case (max) voltage across the primary switch is presented on Figure 24 below.

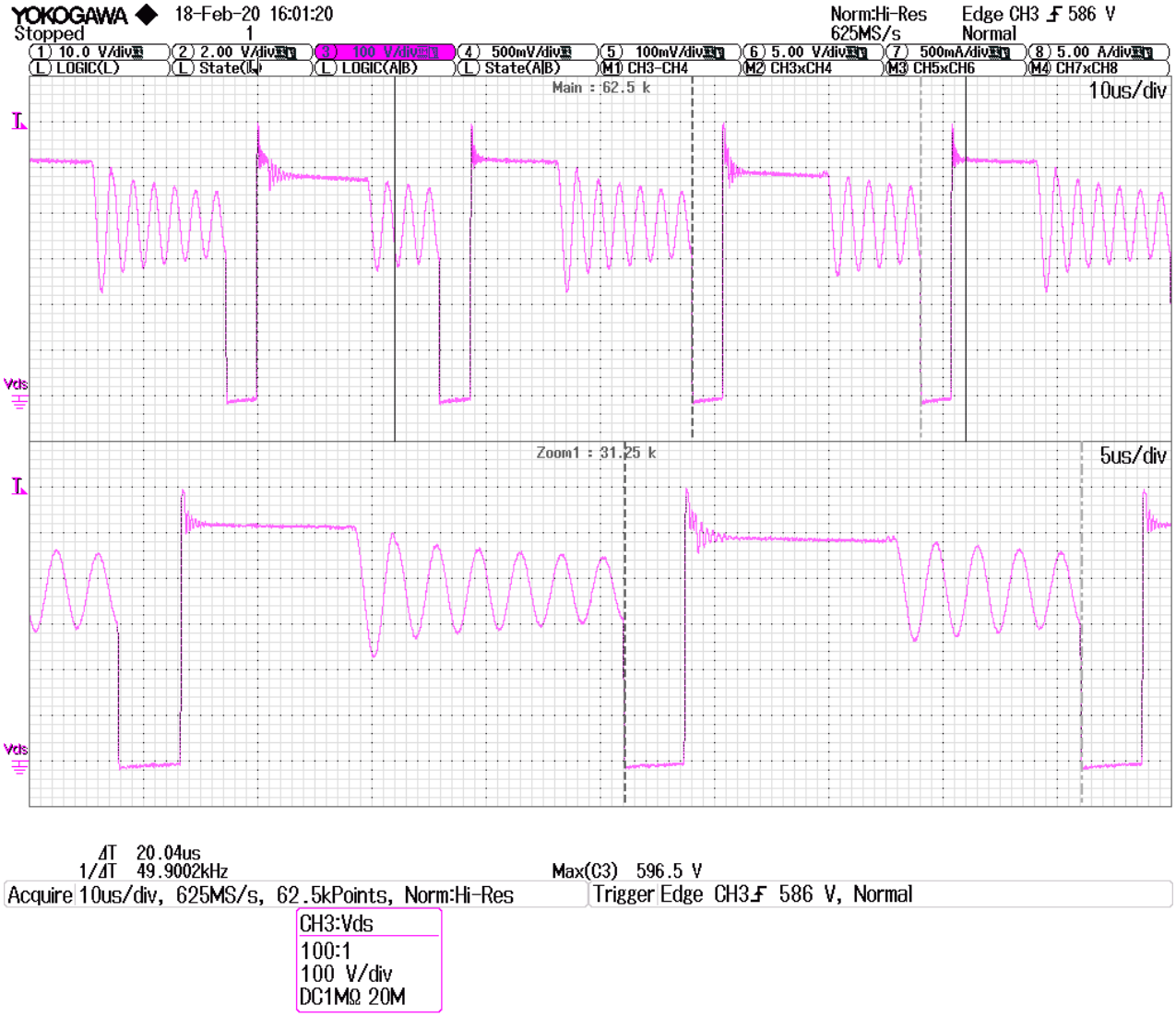

Figure 24 – Primary Switch Worst Case Peak Voltage ($V_{DS(PK)}$ = 596.5 V).

10.8.2 Primary Switching Frequency

The primary switching frequency of the converter varies depending on line and load conditions. It was measured under full load at minimum line input of 90 VAC. The maximum switching frequency occurs at the minimum DC input (73.6 kHz). Under the same condition averaged over half of the mains cycle the primary switching frequency was 70.9 kHz. Details are shown in Figure 25 and Figure 26.

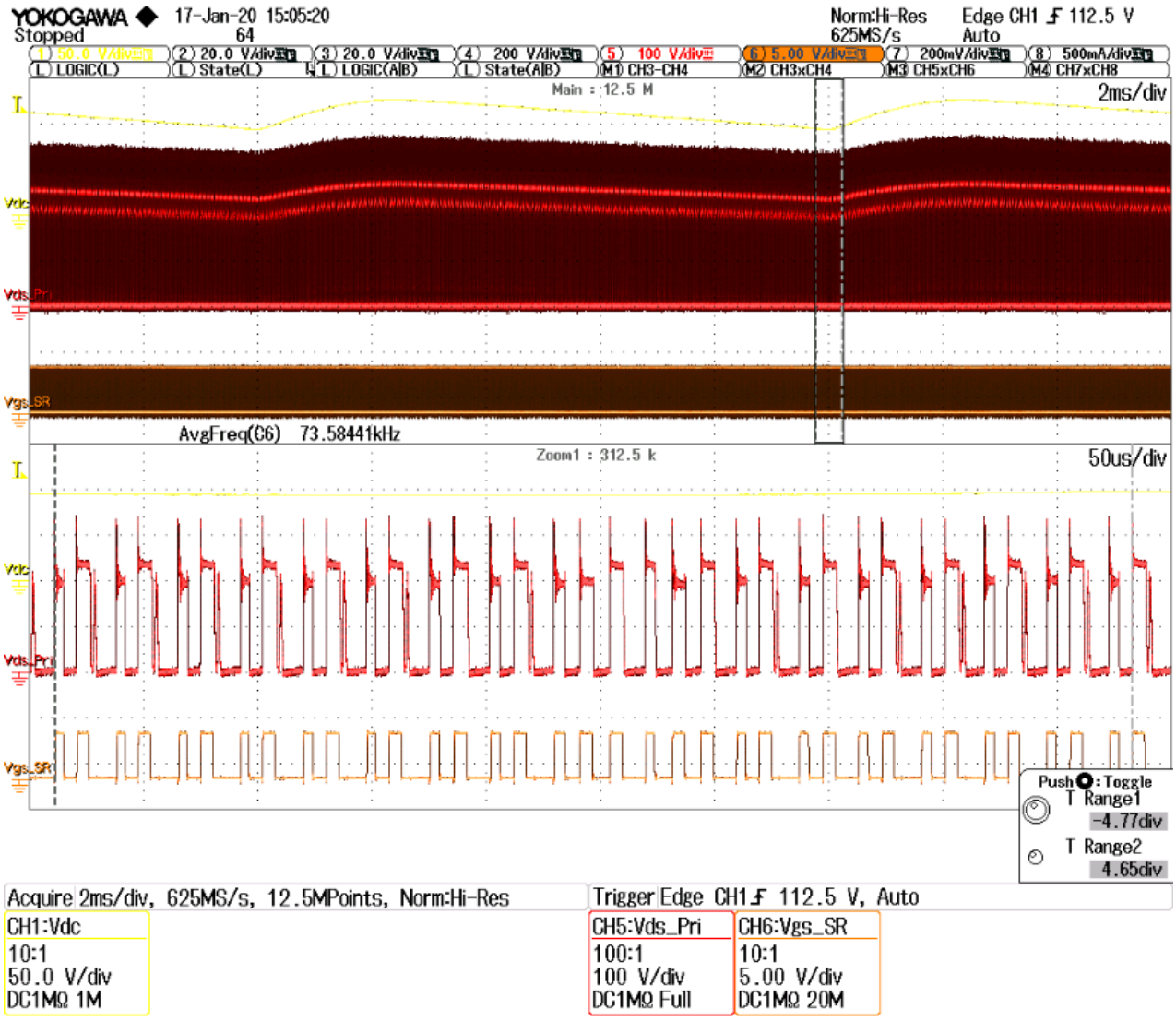

Figure 25 – Max Primary Switching Frequency (73.6 kHz). (CH5 – Primary Switch D-S Voltage; CH6 – SR Gate Drive Signal).

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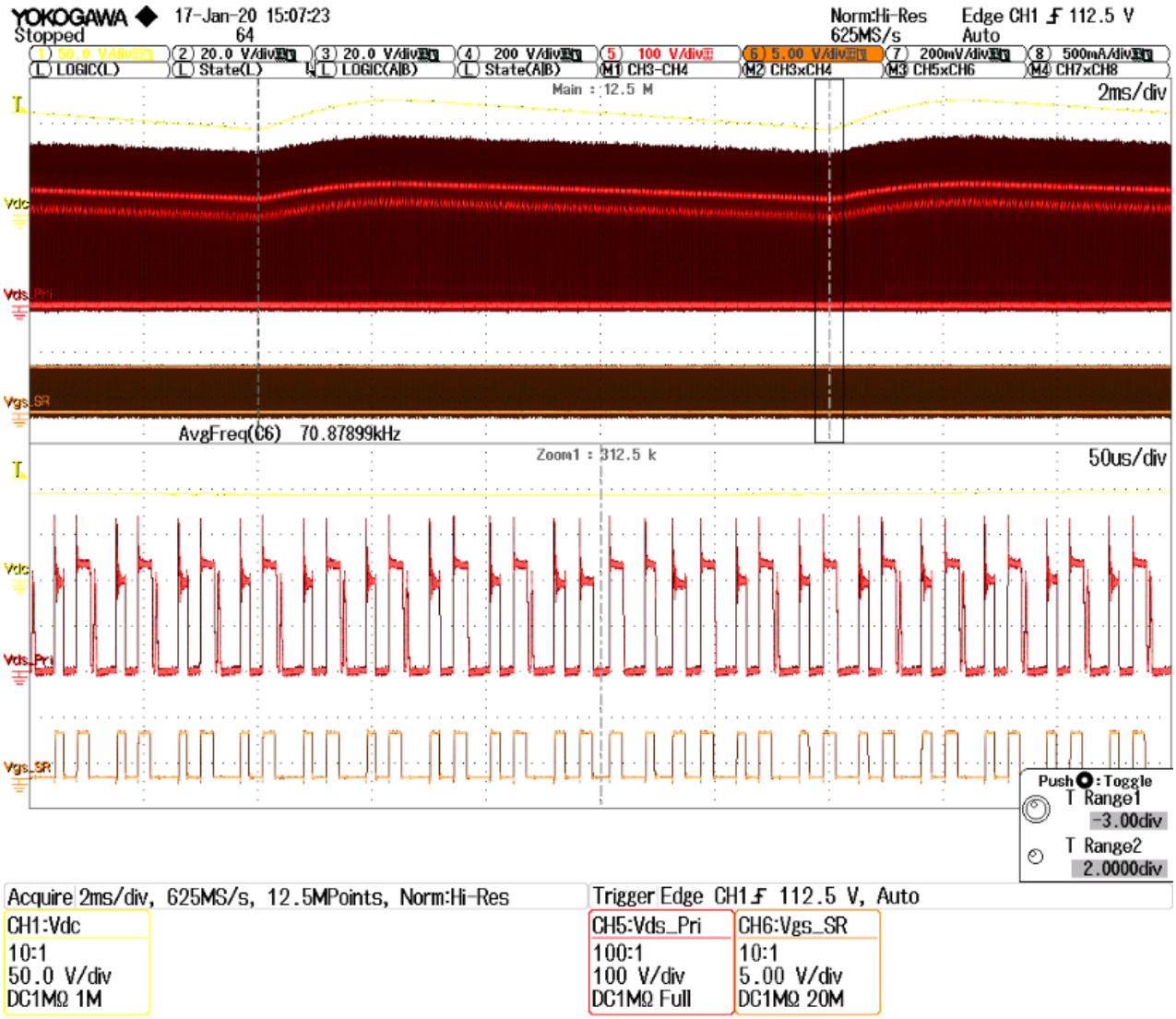

Figure 26 – Average Primary Switching Frequency (70.9 kHz), (CH5 – Primary Switch D-S Voltage; CH6 – SR Gate Drive Signal).

10.8.3 Transformer Current Waveforms

CH1	Primary Switch V_{DS}
CH2	Primary Current
CH3	SR Current
CH4	ICV1
CH5	ICV2
CH6	ILED

Table 4 – Scope Channel Allocation (This Section).

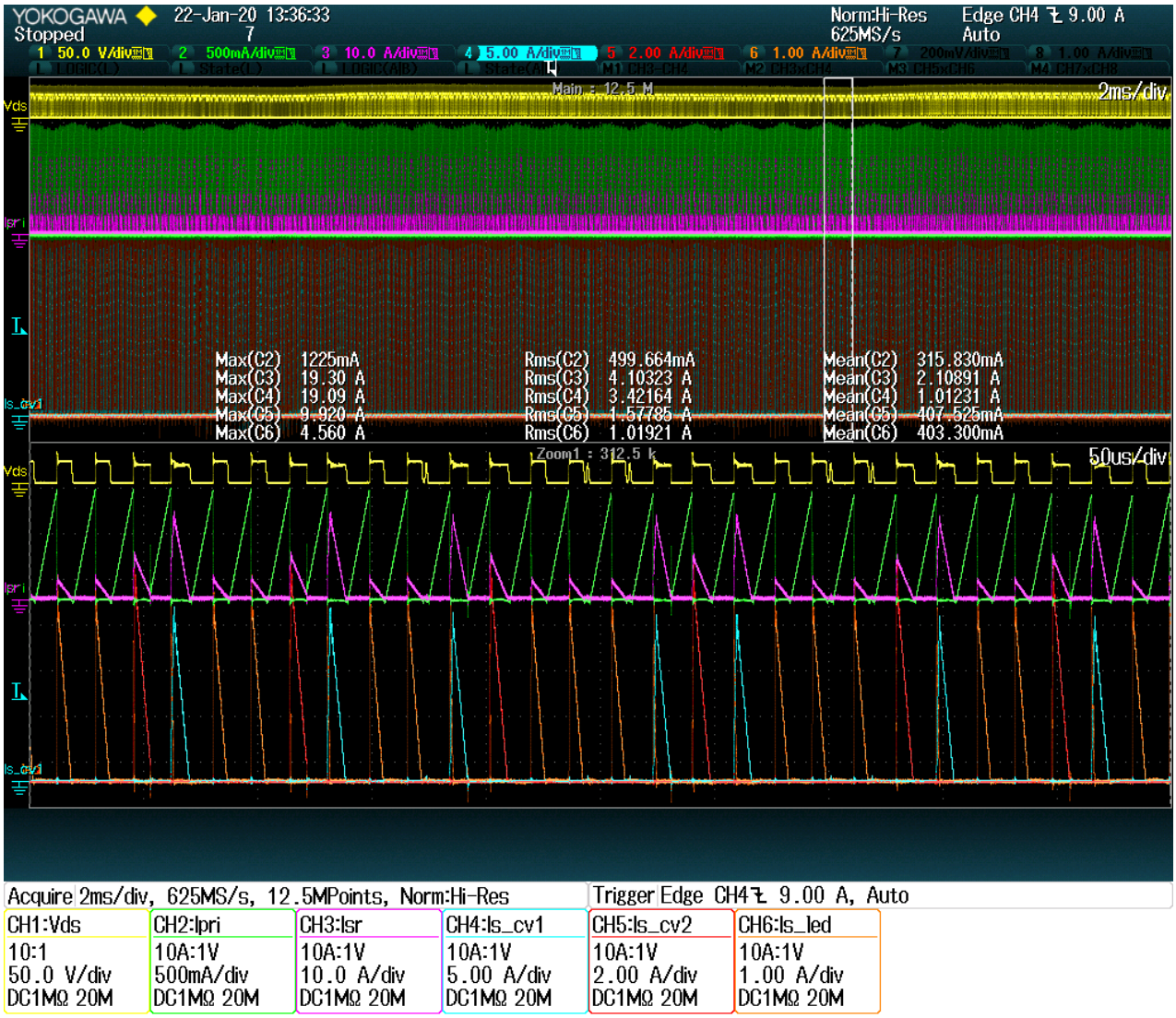

Figure 27 – Transformer All Winding Currents at Minimum Input Voltage.

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		I_{PK} [A]	I_{RMS} [A]	I_{AVG} [A]
Primary	**CH2**	1.23	0.50	0.32
SR	**CH3**	19.3	4.10	2.11
ICV1	**CH4**	19.1	3.42	1.01
ICV2	**CH5**	9.92	1.58	0.41
ILED	**CH6**	4.56	1.02	0.40

Table 5 – Figure 27 current values

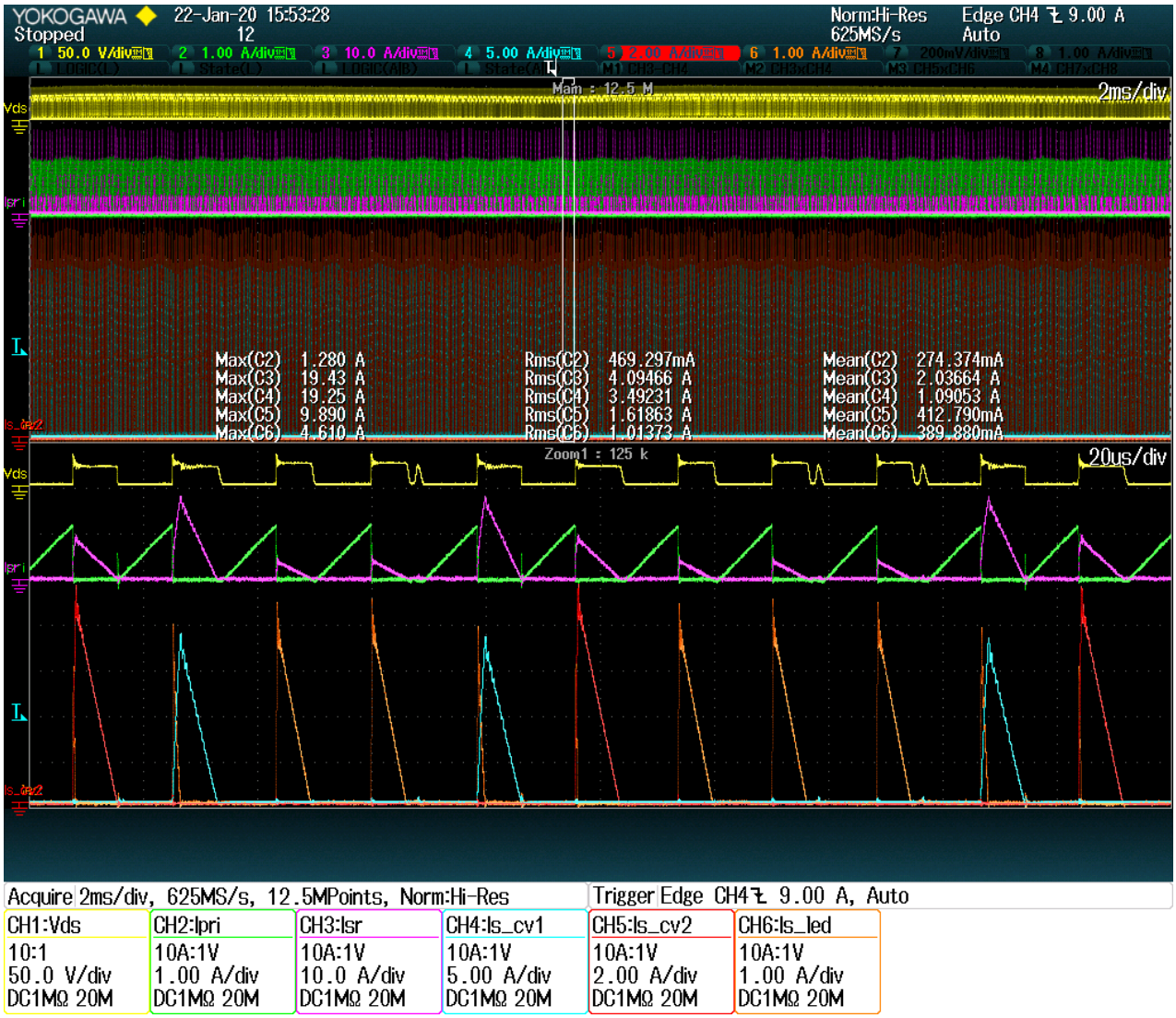

Figure 28 – Transformer All Winding Currents at Minimum Input Voltage, Showing Winding RMS Current Over a Mains Half Cycle.

		I_{PK} [A]	I_{RMS} [A]	I_{AVG} [A]
Primary	**CH2**	1.28	0.47	0.27
SR	**CH3**	19.4	4.09	2.04
ICV1	**CH4**	19.3	3.49	1.09
ICV2	**CH5**	9.89	1.62	0.41
ILED	**CH6**	4.61	1.01	0.39

Table 6 – Figure 28 Current Values.

Figure 29 – Transformer Currents – Detailed View.

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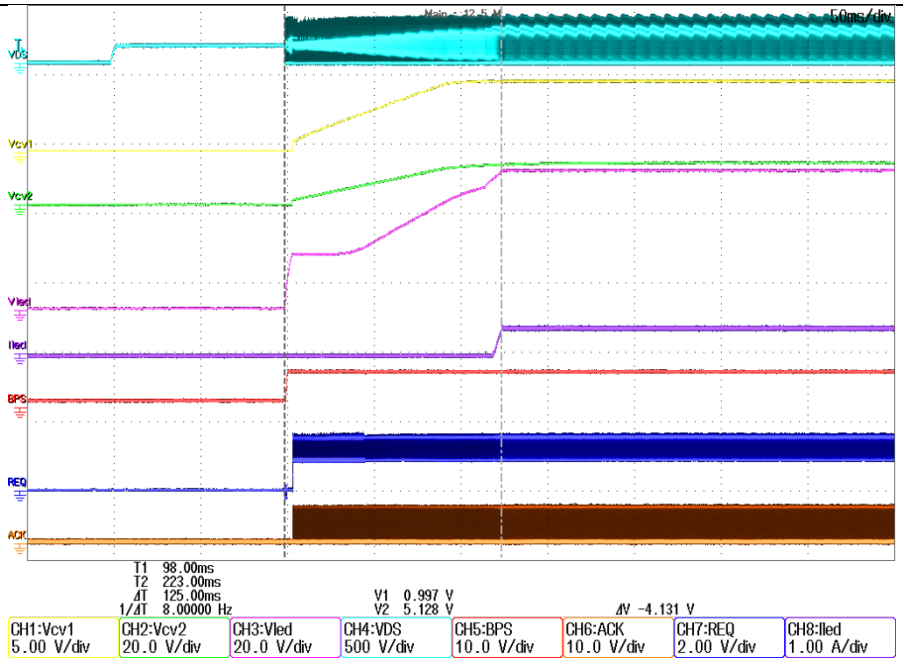
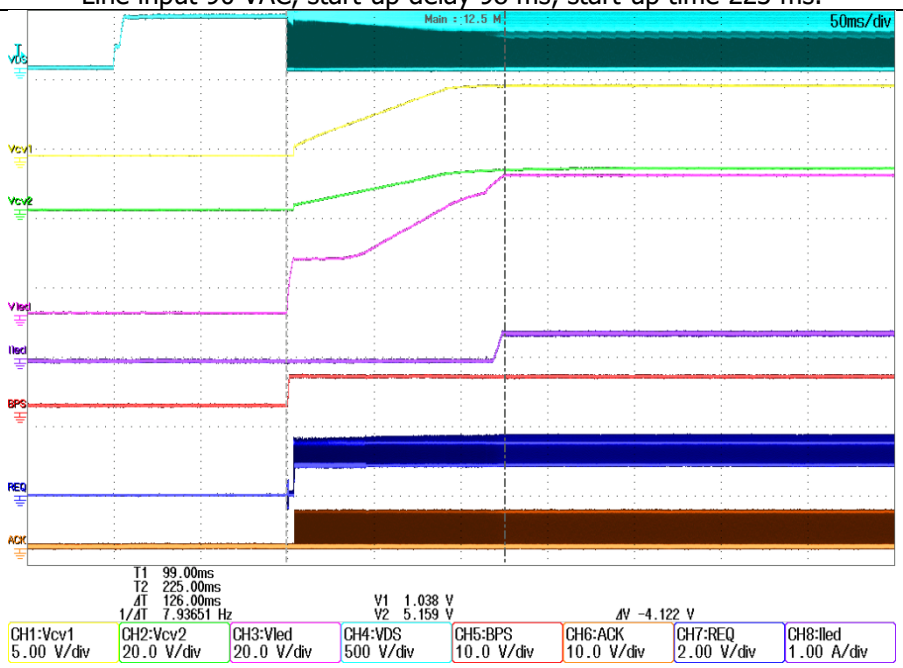
10.9 *Start-Up*

10.9.1 Full Load Start-up



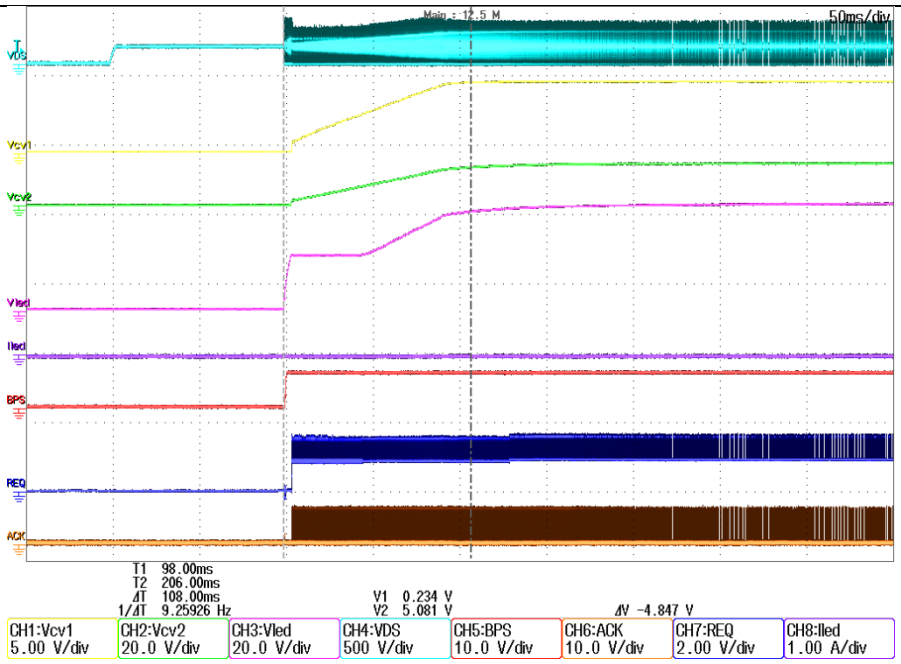
Line input 90 VAC, start-up delay 98 ms, start-up time 223 ms.



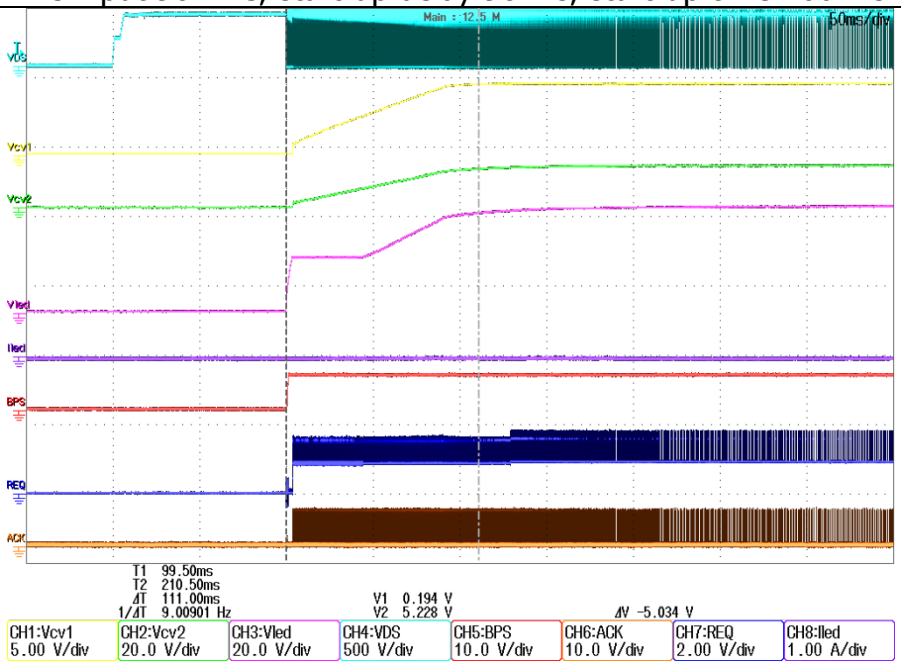
Line input 265 VAC, start-up delay 99 ms, start-up time 225 ms.

Figure 30 – Full Load Start-up.

10.9.2 No-Load Start-up



Line input 90 VAC, start-up delay 98 ms, start-up time 206 ms.



Line input 265 VAC, start-up delay 100 ms, start-up time 210 ms.

Figure 31 – No-load Start-up.

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10.9.3 Start-up Under CV1 Fault Conditions

CH1	VCV1
CH2	VCV2
CH3	VLED
CH4	Vin_DC
CH6	LED_RET
CH8	Line Current

Table 7 – Scope Channel Allocation (This Section).

10.9.3.1 Start-up Under CV1 Fault Conditions

The converter was tested for start-up under two types of single fault conditions, namely:

- Short circuit to GND at one of the main outputs;
- Feedback pin on InnoMux shorted to GND (one output at a time)

In all cases, the converter protection prevented any permanent damage to its components. The peak line current did not exceed 0.5 A. The line fuse F1 remained intact. The converter went into auto restart for the duration of the fault condition. It resumed normal operation after the fault condition was removed. With the feedback signal absent controller went into auto restart before the CV1 and CV2 outputs reach regulation. With the feedback signal form the LED output missing the LED output reached its OVP level. This level is set to approximately 120% of regulation. Details of the start-up behavior under those fault conditions are shown in Figure 32 to Figure 49.

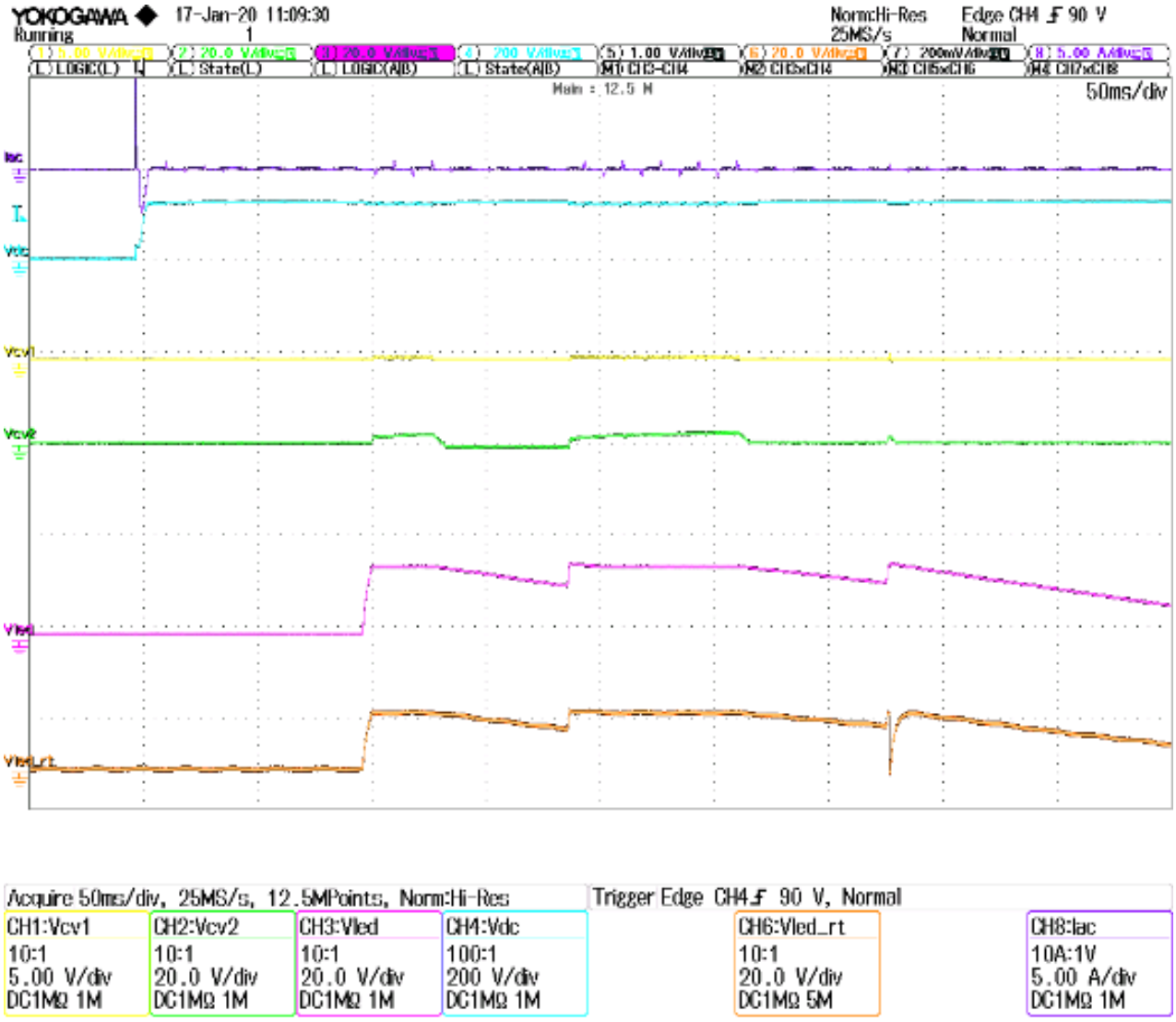

Figure 32 – Start-up With CV1 Shorted to GND. Line Input 90 V.

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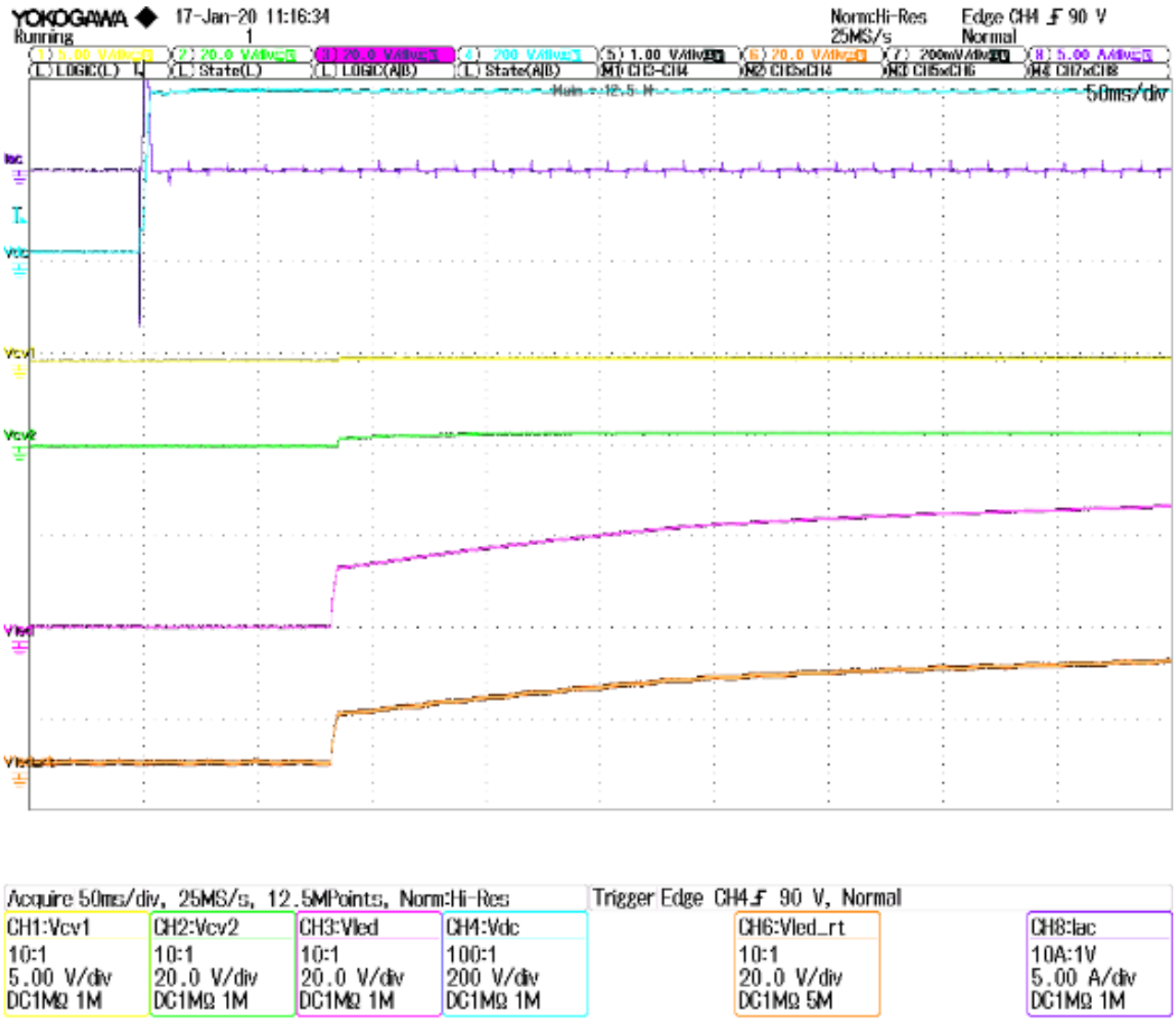

Figure 33 – Start-up With CV1 Shorted to GND. Line Input 265 V.

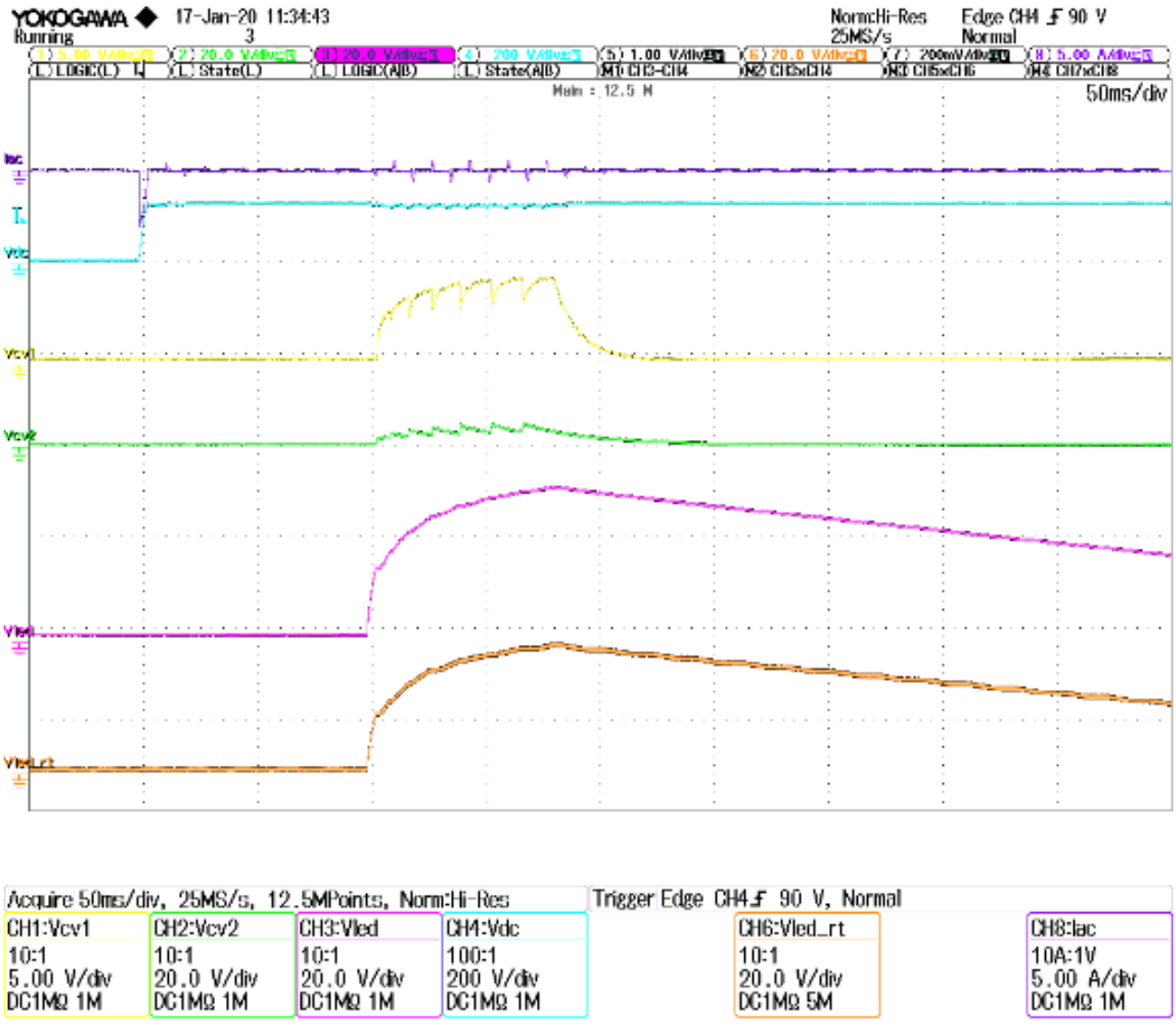

Figure 34 – Start-up With No Feedback for CV1; Line Input 90 V.

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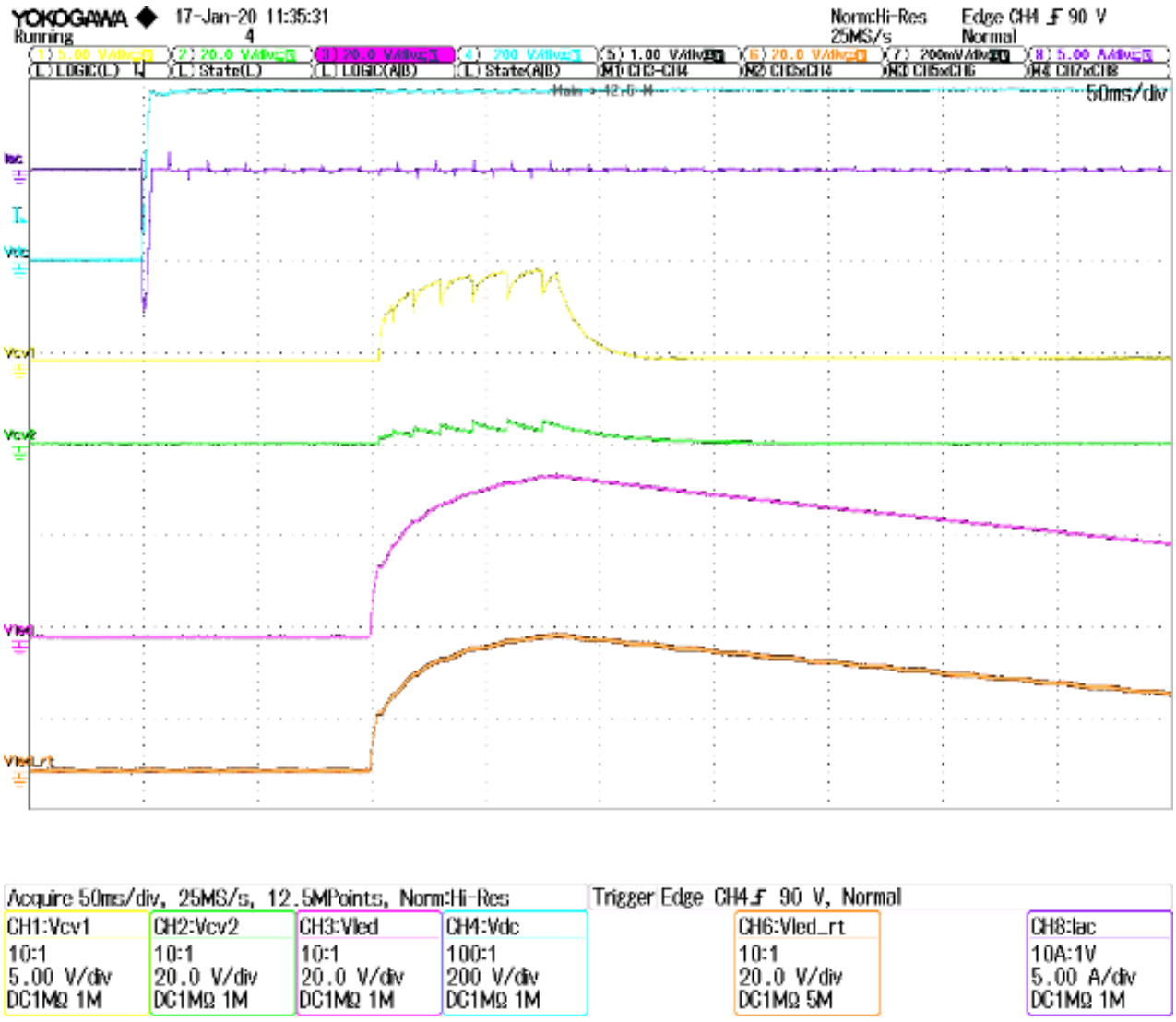

Figure 35 – Start-up With No Feedback for CV1; Line Input 265 V.

10.9.3.2 Start-up Under CV2 Fault Conditions

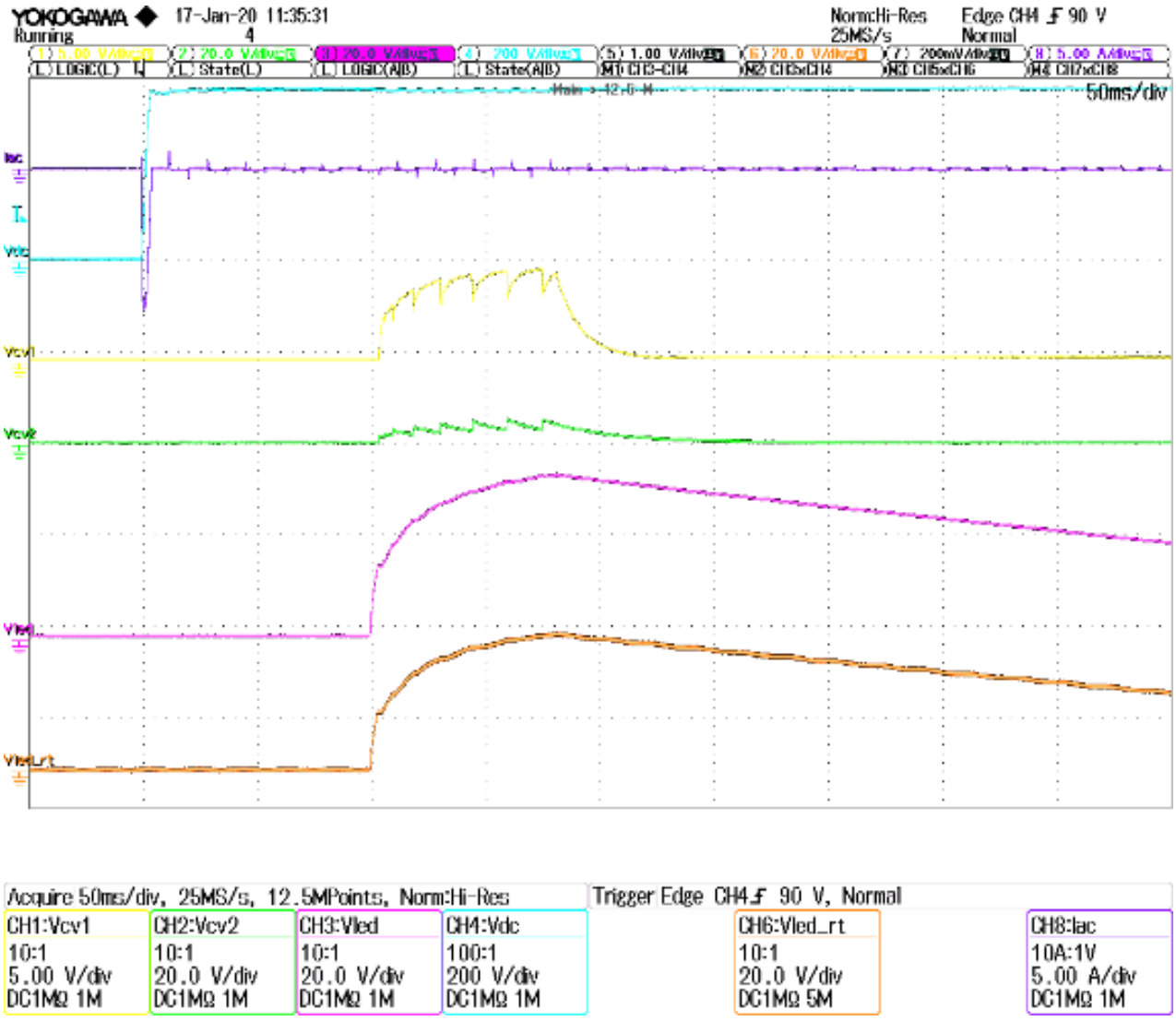

Figure 36 – Start-up With CV2 Shorted to GND. Line Input 90 V.

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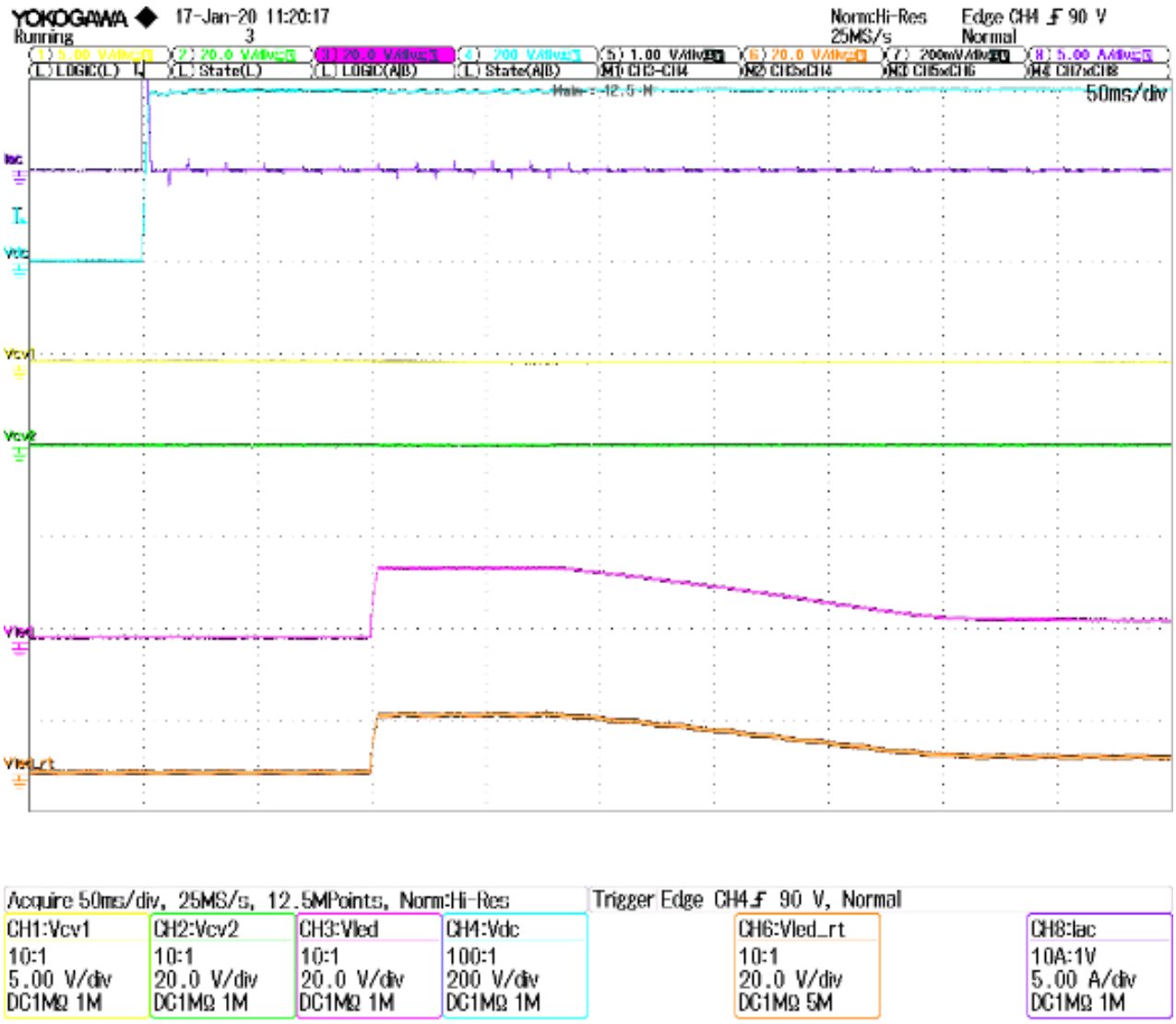

Figure 37 – Start-up With CV2 Shorted to GND. Line Input 265 V.

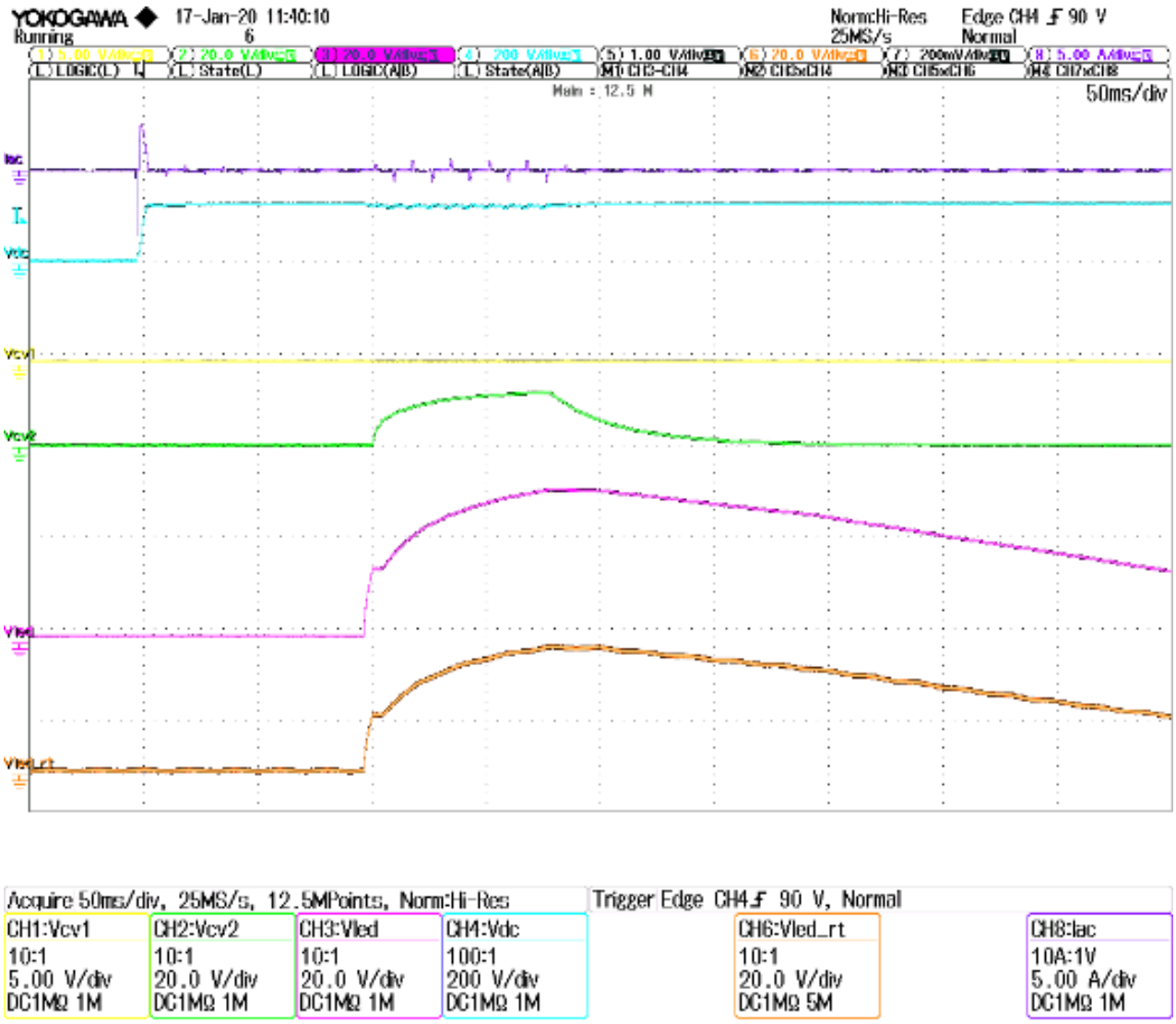

Figure 38 – Start-up With No Feedback for CV2; Line Input 90 V.

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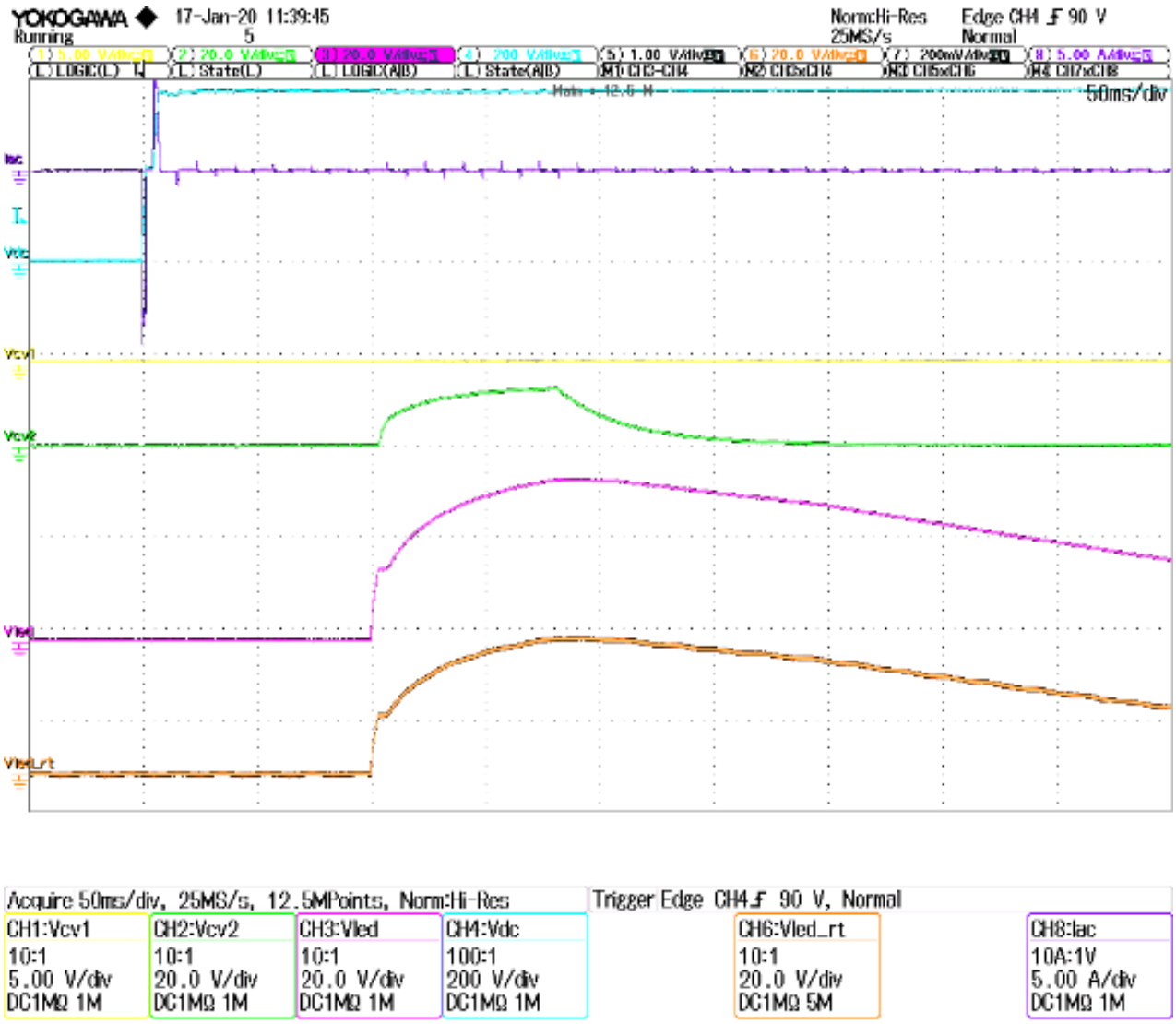

Figure 39 – Start-up With No Feedback for CV2; Line Input 265 V.

10.9.3.3 Start-up Under LED Fault Conditions

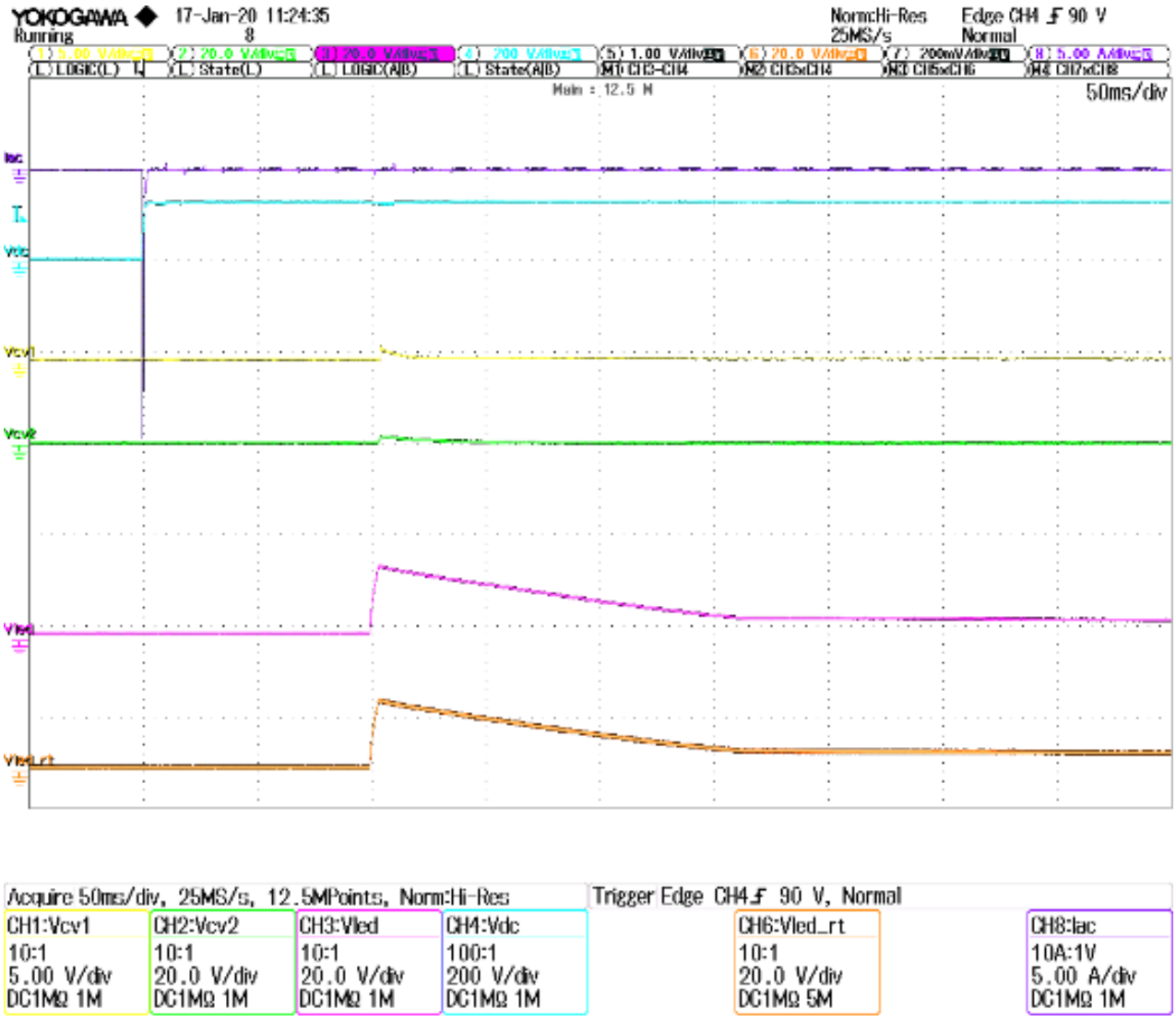

Figure 40 – Start-up With LED Output Shorted to GND. Line Input 90 V.

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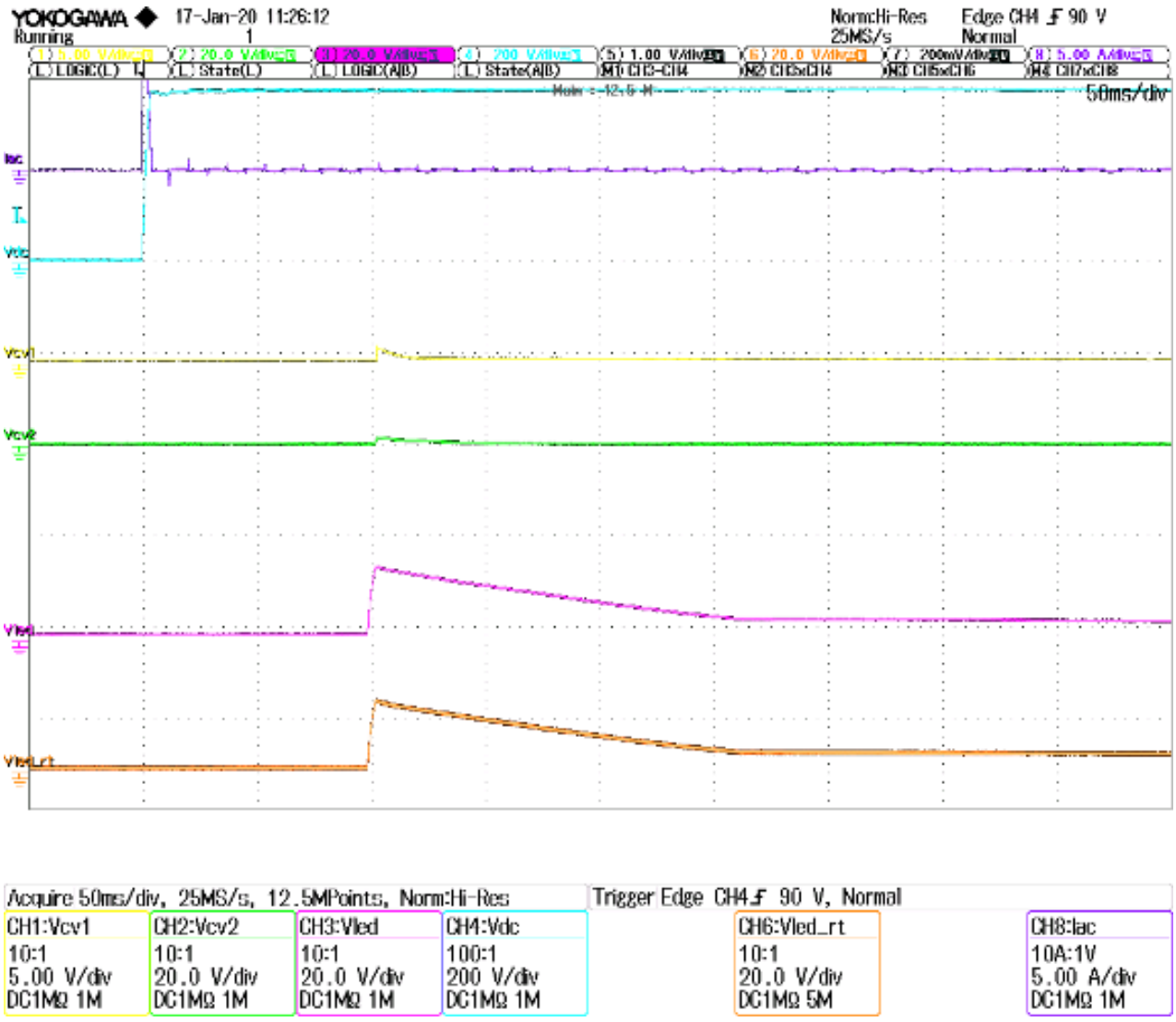

Figure 41 – Start-up With LED Output Shorted to GND. Line Input 265 V.

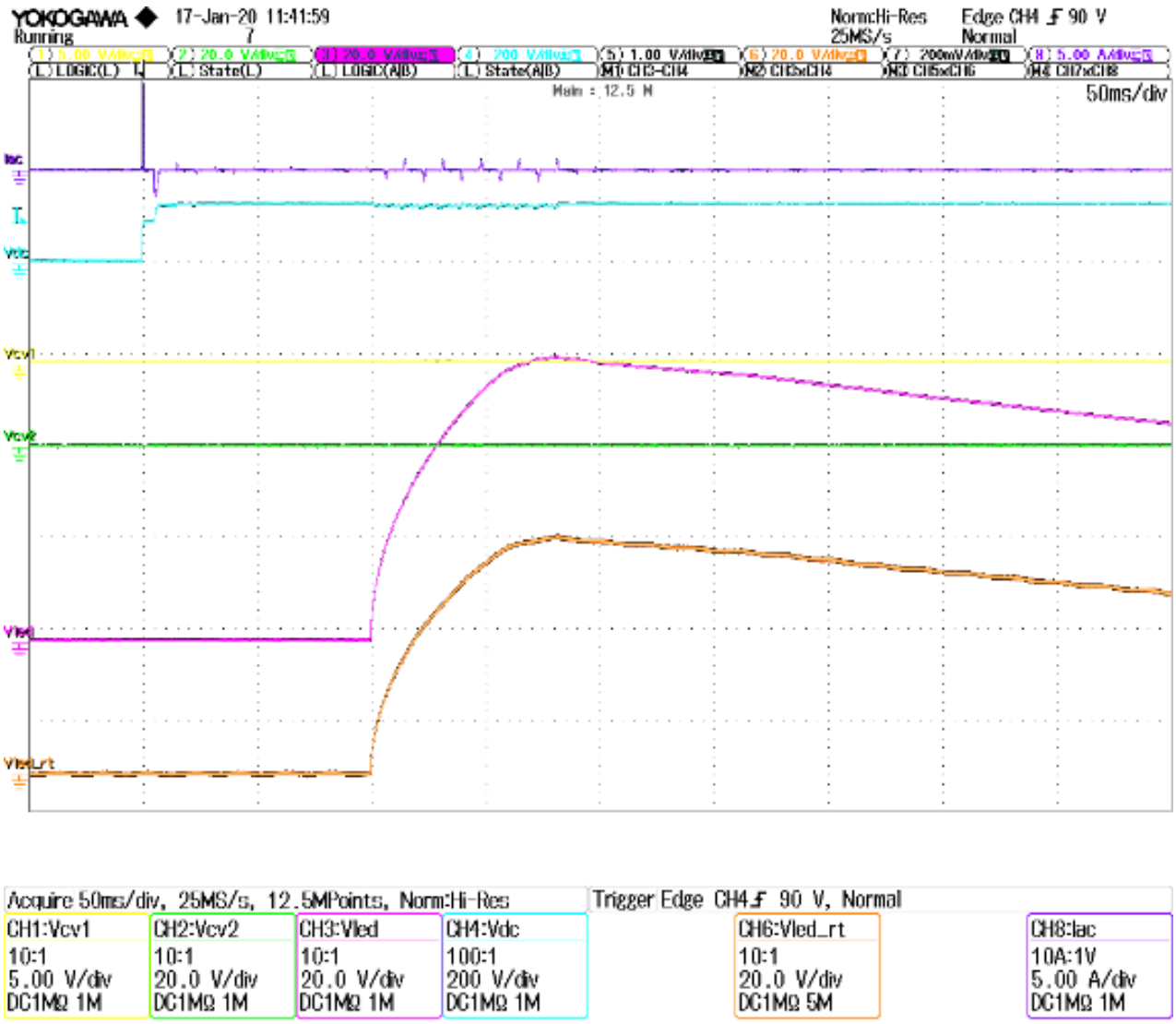

Figure 42 – Start-up With No Feedback From LED Output. Line Input 90 V.

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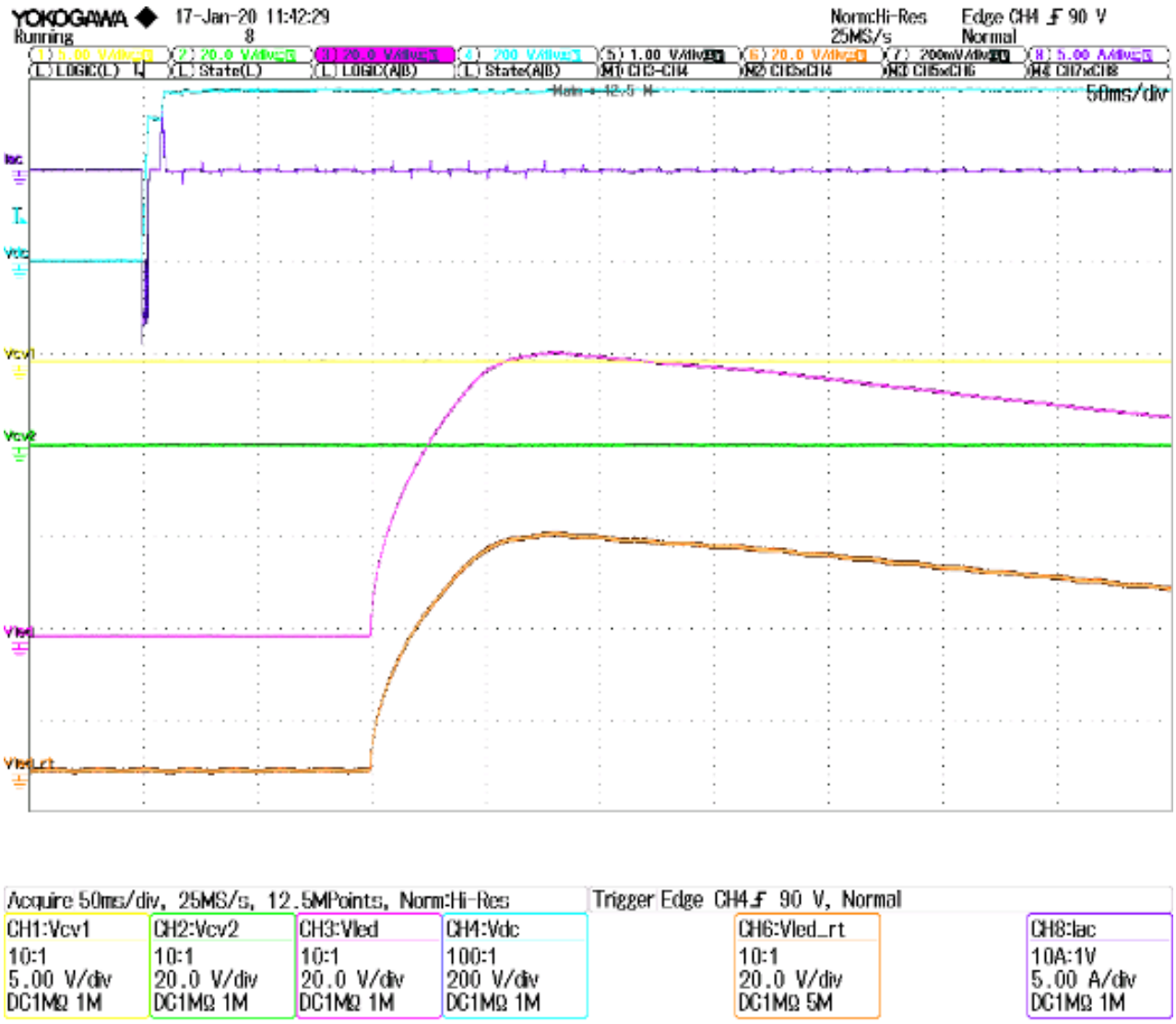

Figure 43 – Start-up With No Feedback From LED Output. Line Input 265 V.

10.10 *Devices Peak Voltages*

10.10.1 SR Worst Case D-S Voltage

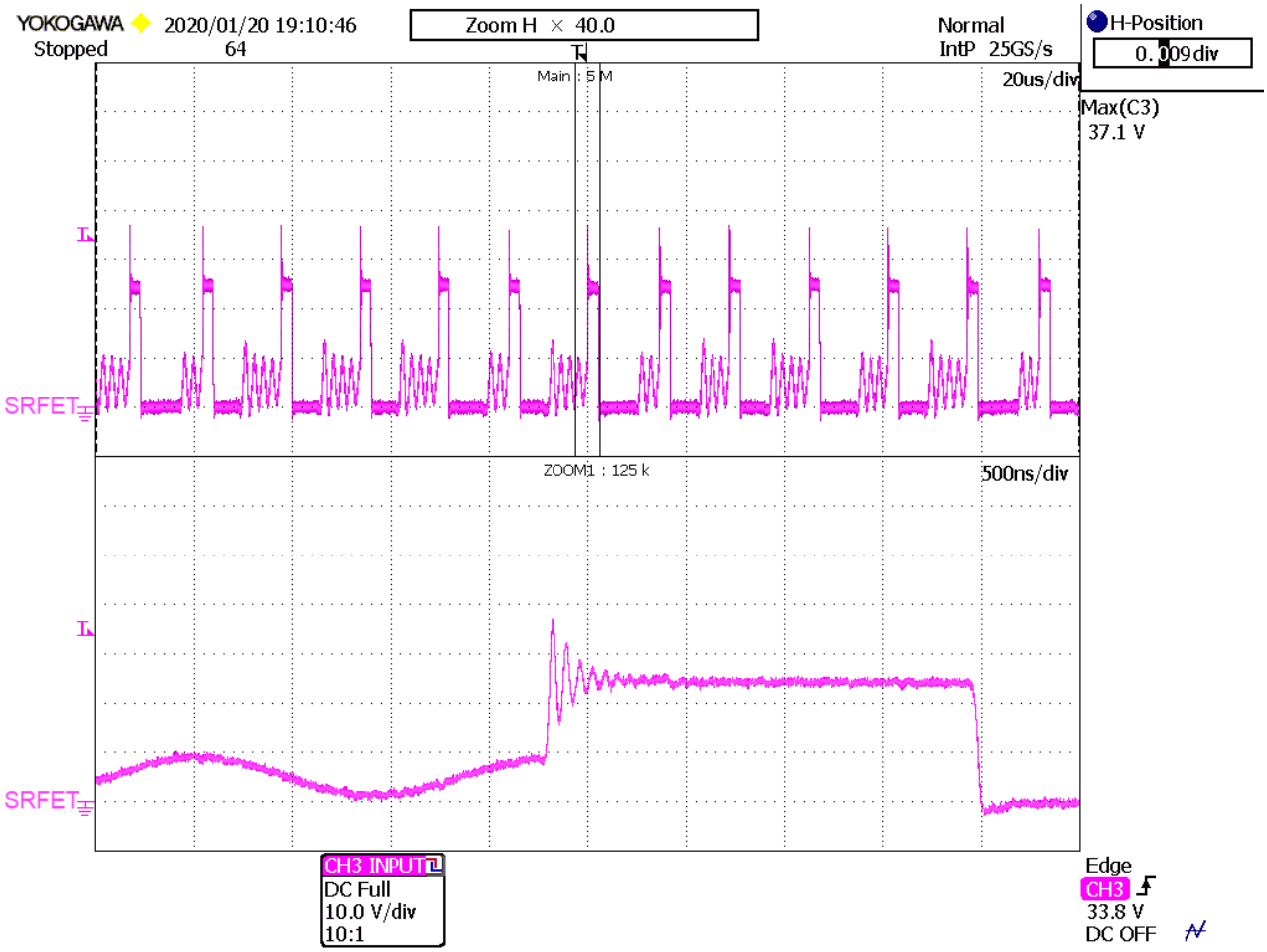

Figure 44 – SR (Q1) D-S Voltage Under Full Load at 375 VDC.

Maximum D-S voltage across the SR FET is 37.1 V.

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10.10.2 CV1 Selection FET Maximum Voltage

Figure 45 – CV1 Selection FET (Q2) D-S Voltage Under Full Load at 375 VDC.

The maximum D-S voltage across the selection FET of CV1 is 5.62 V.

10.10.3 CV2 Selection FET D-S Voltage

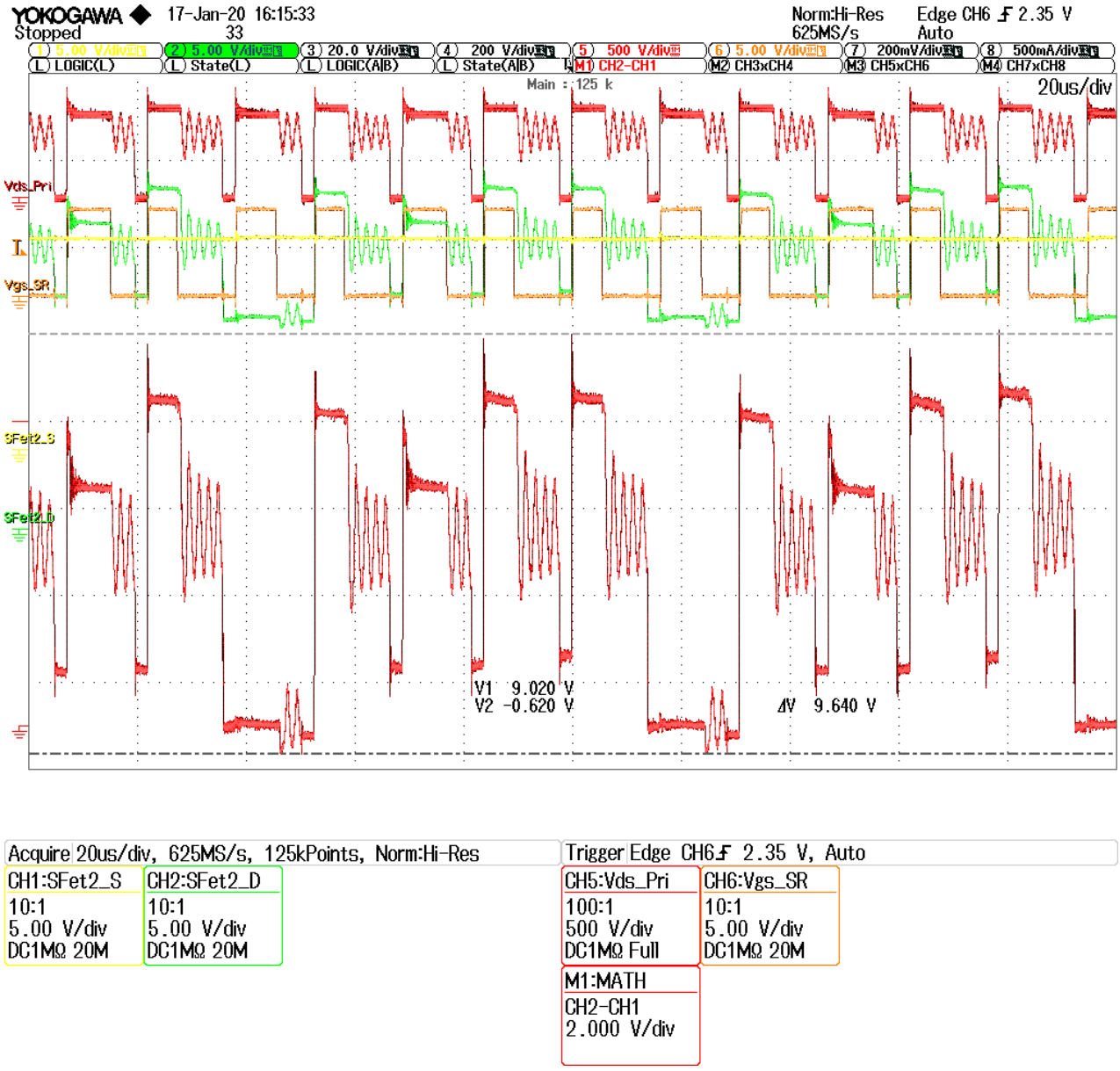

Figure 46 – CV2 Selection FET Under Full Load at 375 VDC Line Voltage.

The maximum D-S voltage across the CV2 selection FET (Q4) is 9.02 V.

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10.10.4 CV2 Blocking Diode Peak Reverse Voltage

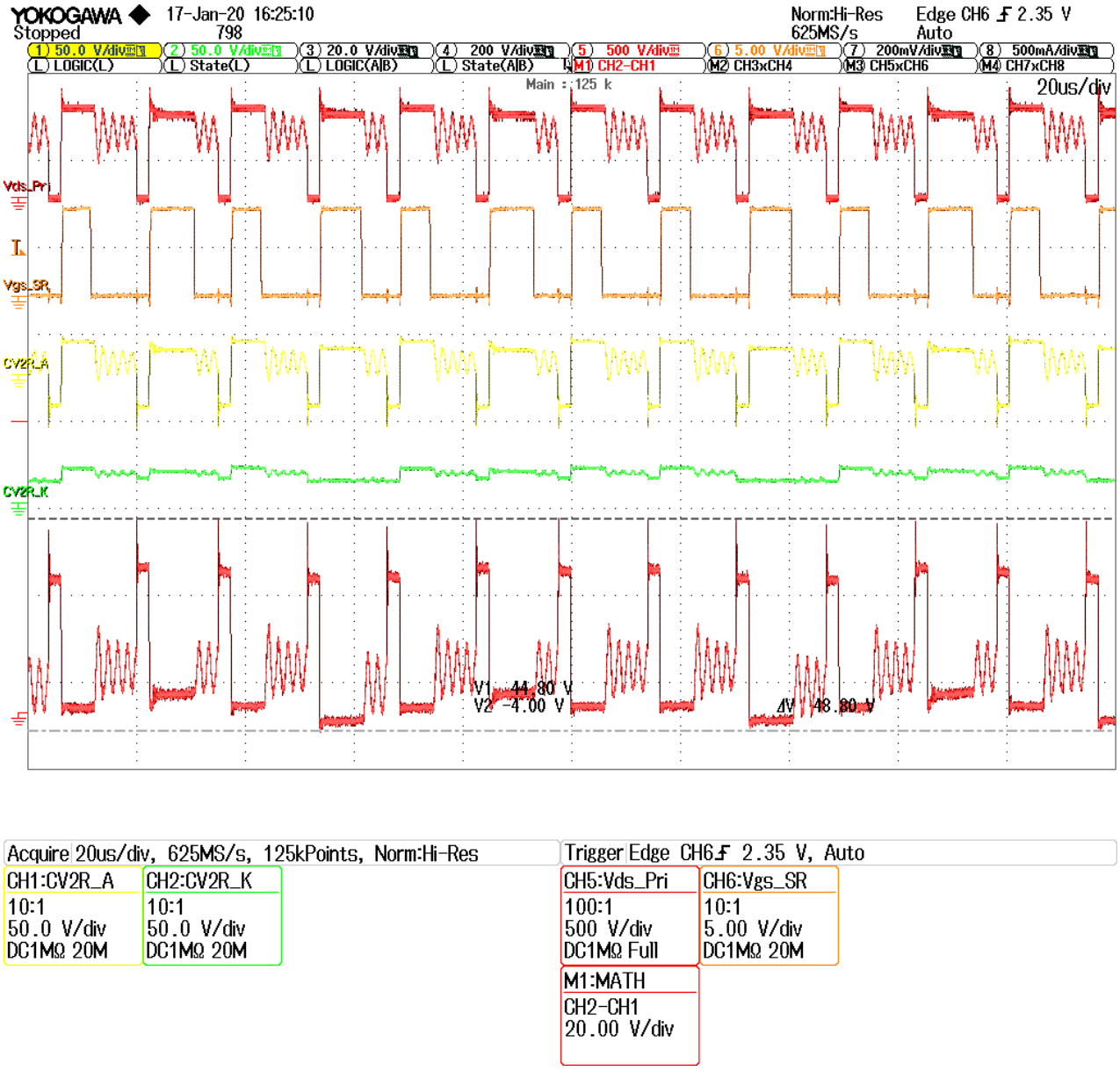

Figure 47 – CV2 Diode Reverse Voltage Under Full Load at 375 VDC.

The worst-case peak reverse voltage across CV2 blocking diode (D5) is 44.8 V.

10.10.5 LED Rectifier Diode Reverse Voltage under Full Load at 375 VDC

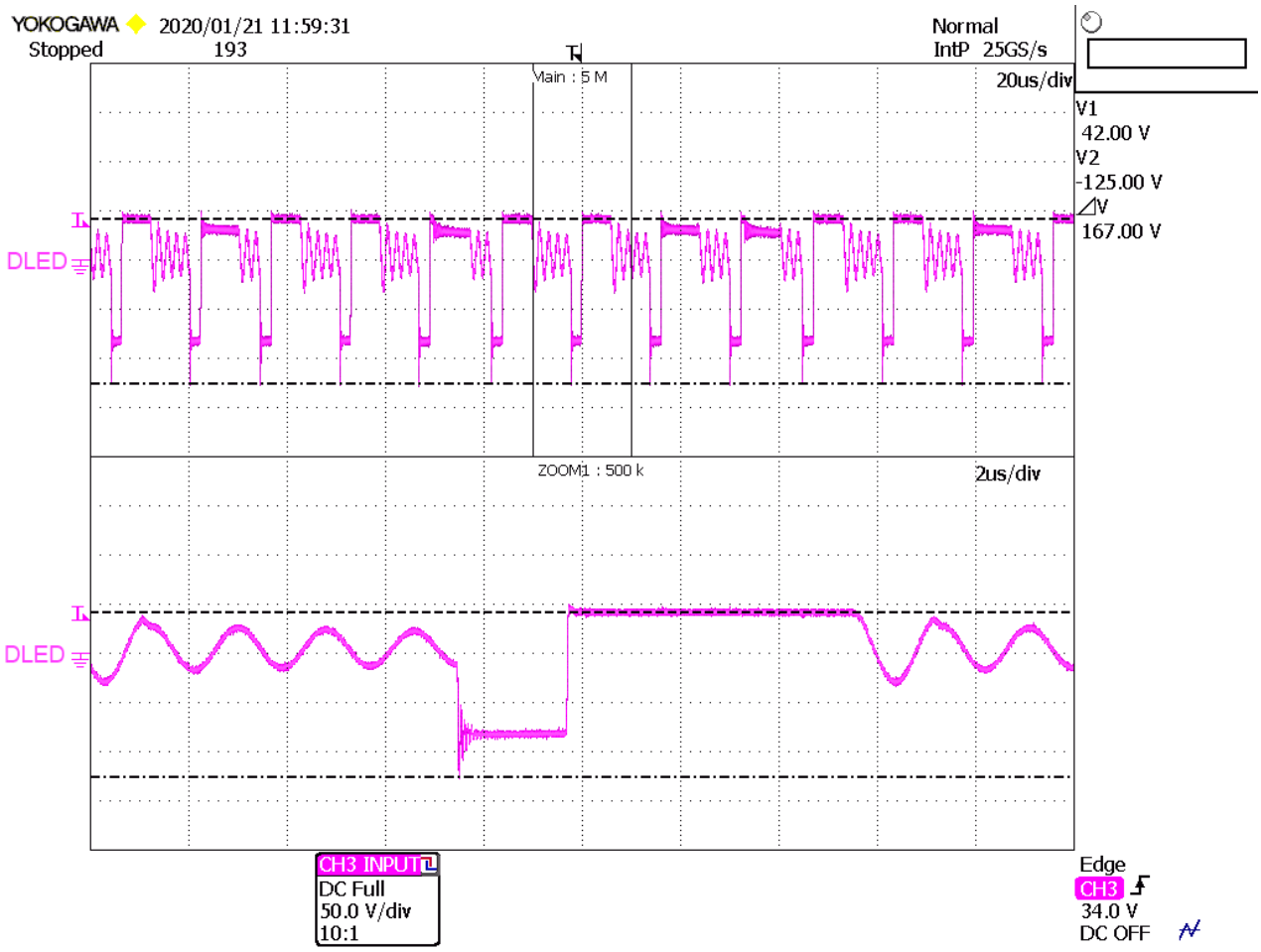

Figure 48 – Voltage on LED Diode Under Full Load at 375 VDC.

The worst-case peak reverse voltage across the LED rectifier diode (D3) is 167 V.

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10.11 *Brown – Out and Brown - In*

The Brown In and Brown Out results were measured at fill load on all outputs. The results are shown in the table below. Screenshots illustrating the tests are shown in Figure 49.

Brown Out Threshold	Brown In Threshold
[V_{RMS}]	[V_{RMS}]
77	78.2

Table 8 – Brown-In and Brown-Out Thresholds at Full power.

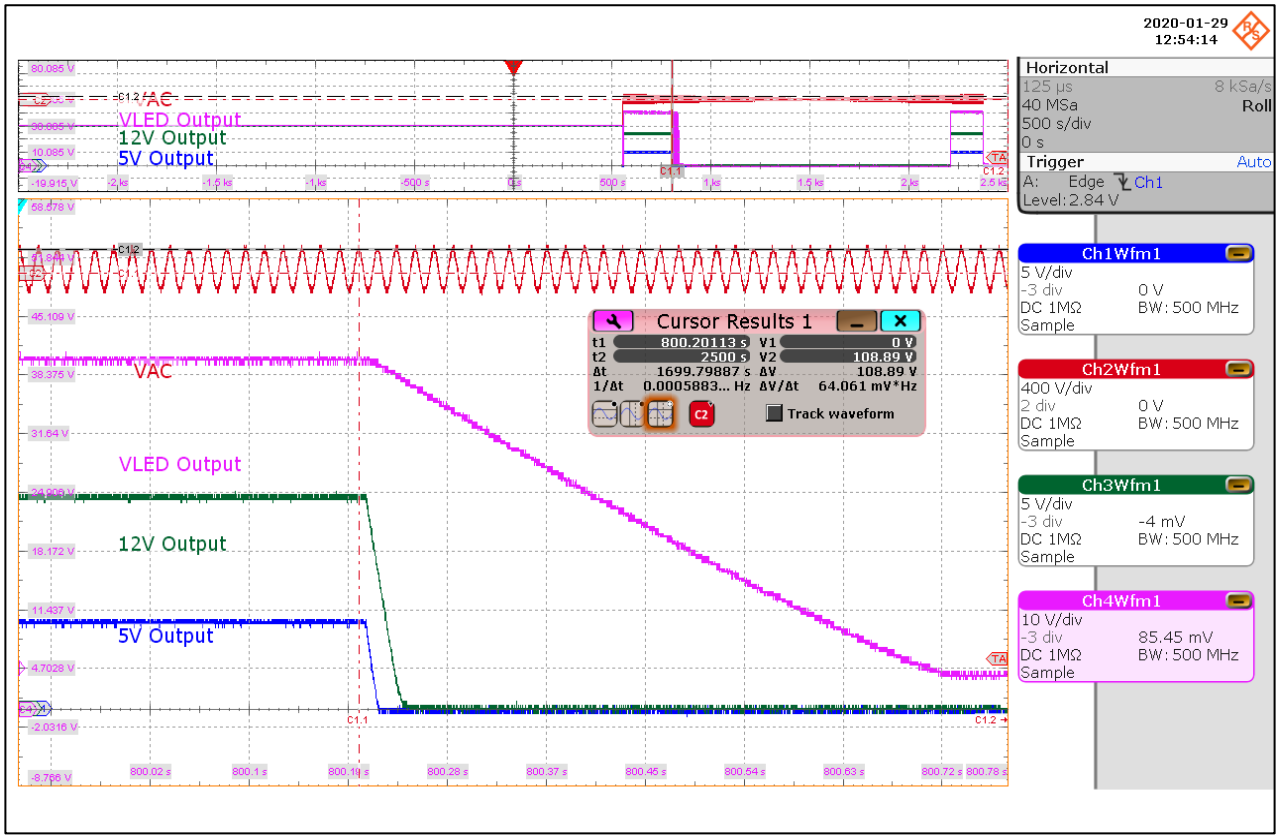

Figure 49 – Brown-Out Response at Full Power.

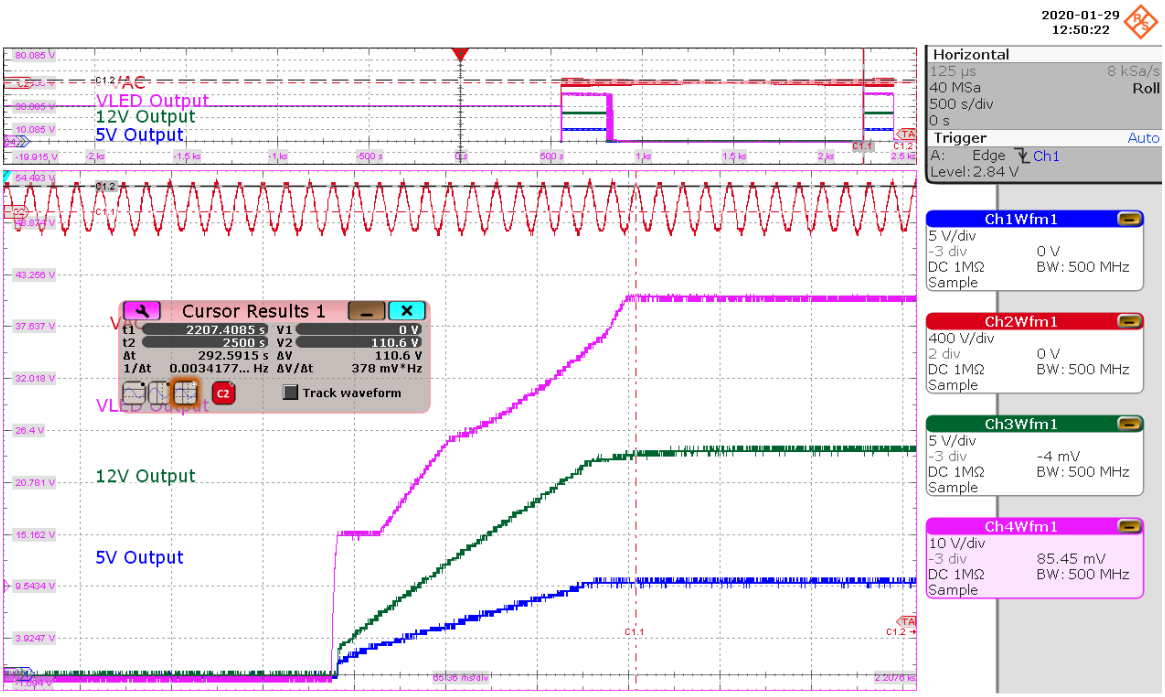

Figure 50 – Brown-In Response at Full Power.

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10.12 *Output Protections*

10.12.1 CV1 Power Limit

The CV1 power limit was tested at line voltage 90 V and 265 V, with LED stack voltages 33 V, 37 V and 40 V. The test results are presented in Table 9. The worst case output current thresholds measured were 2.5 A and 3.3 A accordingly. These tests are illustrated in Figure 51 and Figure 52 below.

V_{IN} [V_{RMS}]	I_{IN} [mA_{RMS}]	P_{IN} [W]	V_CV1 [V_{DC}]	I_CV1 [A_{DC}]	P_CV1 [W]	V_CV2 [V_{DC}]	I_CV2 [A_{DC}]	P_CV2 [W]	V_LED [V_{DC}]	I_LED [mA_{DC}]	P_LED [W]	P_{OUT} [W]
90	698.2	37.6	4.87	2.6	12.66	11.95	0.42	5.02	33.27	405.3	13.5	31.2
265	333.4	38.2	4.87	3	14.59	11.96	0.42	5.02	33.22	405.7	13.5	33.1
90	714.8	39.1	4.88	2.5	12.21	11.95	0.42	5.02	36.86	405.2	14.9	32.2
265	359.7	41.2	4.86	3.2	15.55	11.97	0.42	5.03	36.84	405.6	14.9	35.5
90	742.9	40.8	4.88	2.5	12.20	11.95	0.42	5.02	40.24	405.1	16.3	33.5
265	377.3	43.4	4.87	3.3	16.05	11.97	0.42	5.03	40.09	405.8	16.3	37.3

Table 9 – CV1 Output Power Limit.

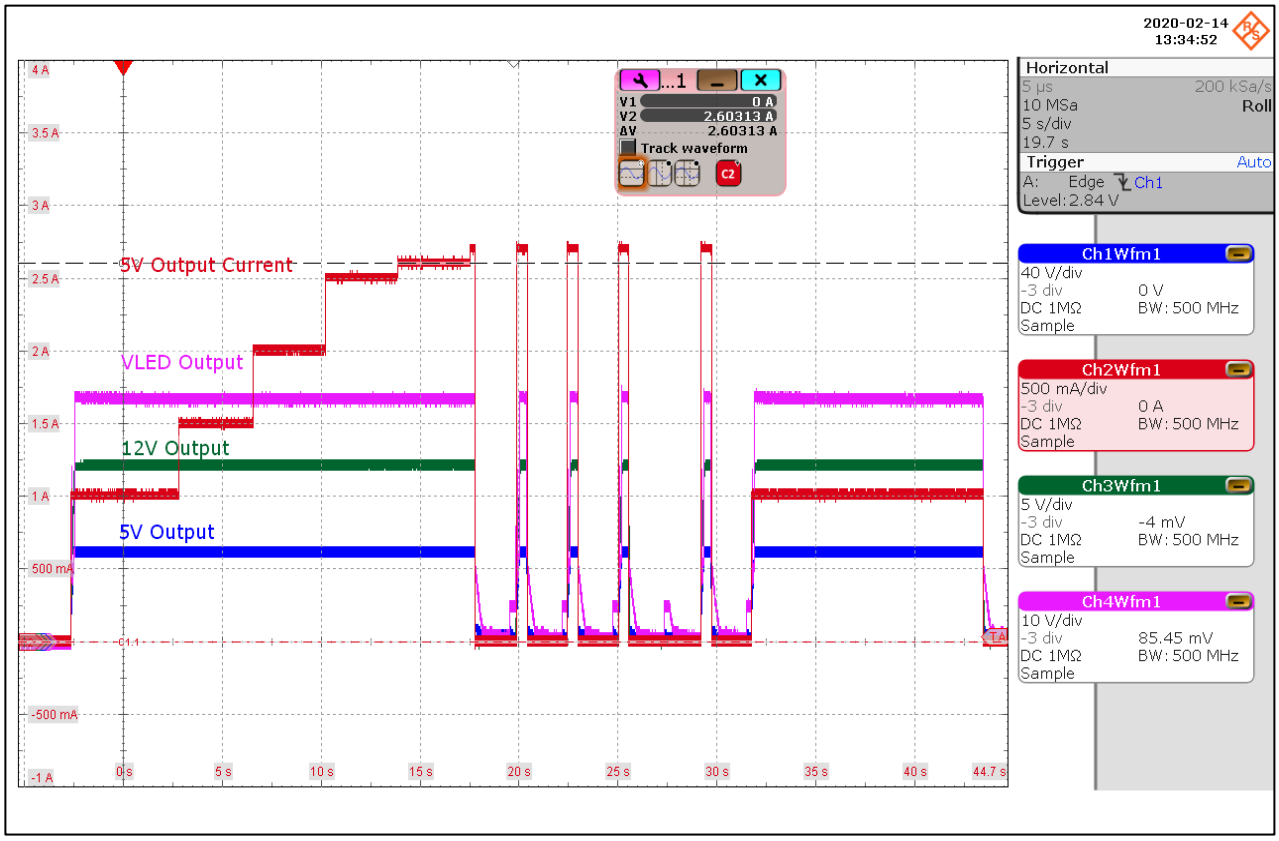

Figure 51 – CV1 Output Power Limit Test (WC) at 90 VAC.

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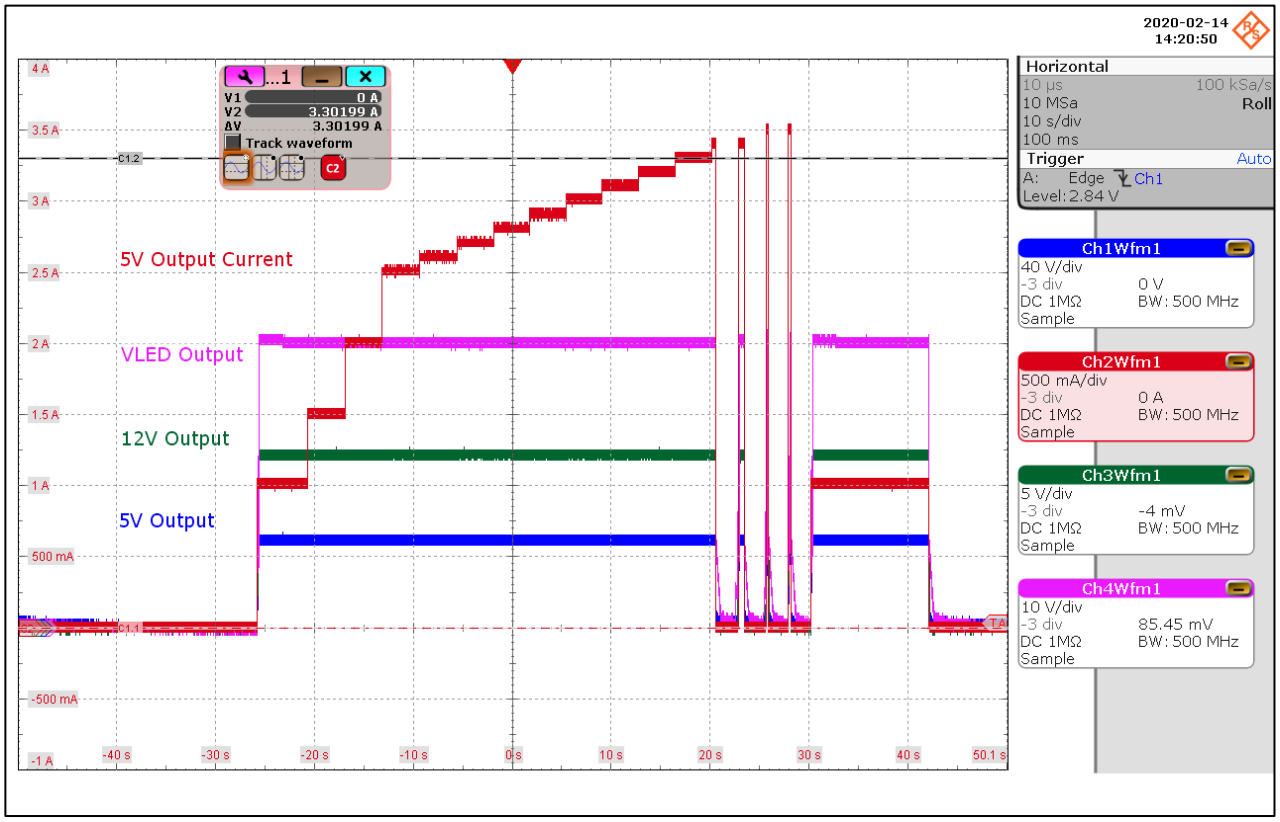

Figure 52 – CV1 Power Limit Test (WC) at 265 VAC.

10.12.2 CV2 Output Power Limit

The CV12 power limit was tested at line voltage 90 V and 265 V, with LED stack voltages 33 V, 37 V and 40 V. The test results are presented in the table below. The worst case output current thresholds measured were 1.13 A and 1.47 A accordingly. These tests are illustrated in Figure 53 and Figure 54 below.

V_{IN} [V_{RMS}]	I_{IN} [mA_{RMS}]	P_{IN} [W]	V_CV1 [V_{DC}]	I_CV1 [A_{DC}]	P_CV1 [W]	V_CV2 [V_{DC}]	I_CV2 [A_{DC}]	P_CV2 [W]	V_LED [V_{DC}]	I_LED [mA_{DC}]	P_LED [W]	P_{OUT} [W]
90	708.0	38.3	4.98	1	4.98	11.85	1.12	13.44	33.22	405.3	13.5	31.9
265	349.6	40.0	5	1	5.00	11.86	1.39	16.44	33.17	405.7	13.5	34.9
90	744.0	40.2	4.99	1	4.99	11.78	1.13	13.36	36.89	405.4	15.0	33.3
265	368.0	42.5	5	1	5.00	11.87	1.43	16.96	36.99	405.3	15.0	37.0
90	760.3	41.4	4.98	1	4.98	11.85	1.09	12.94	40.09	405.6	16.3	34.2
265	391.1	44.6	5	1	5.00	11.88	1.47	17.46	40.02	405.9	16.2	38.7

Table 10 – CV1 Output Power Limit.

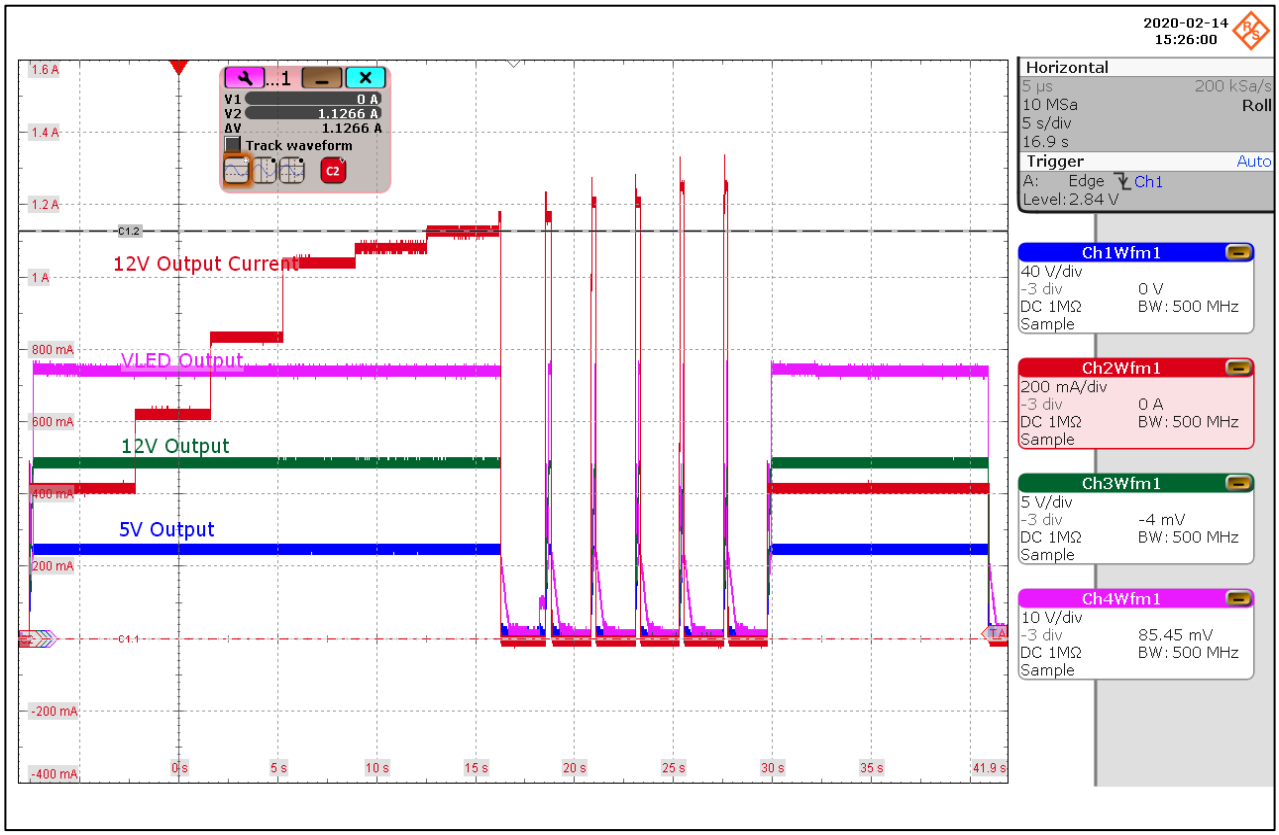

Figure 53 – CV2 Output Power Limit Test (WC) at 90 VAC.

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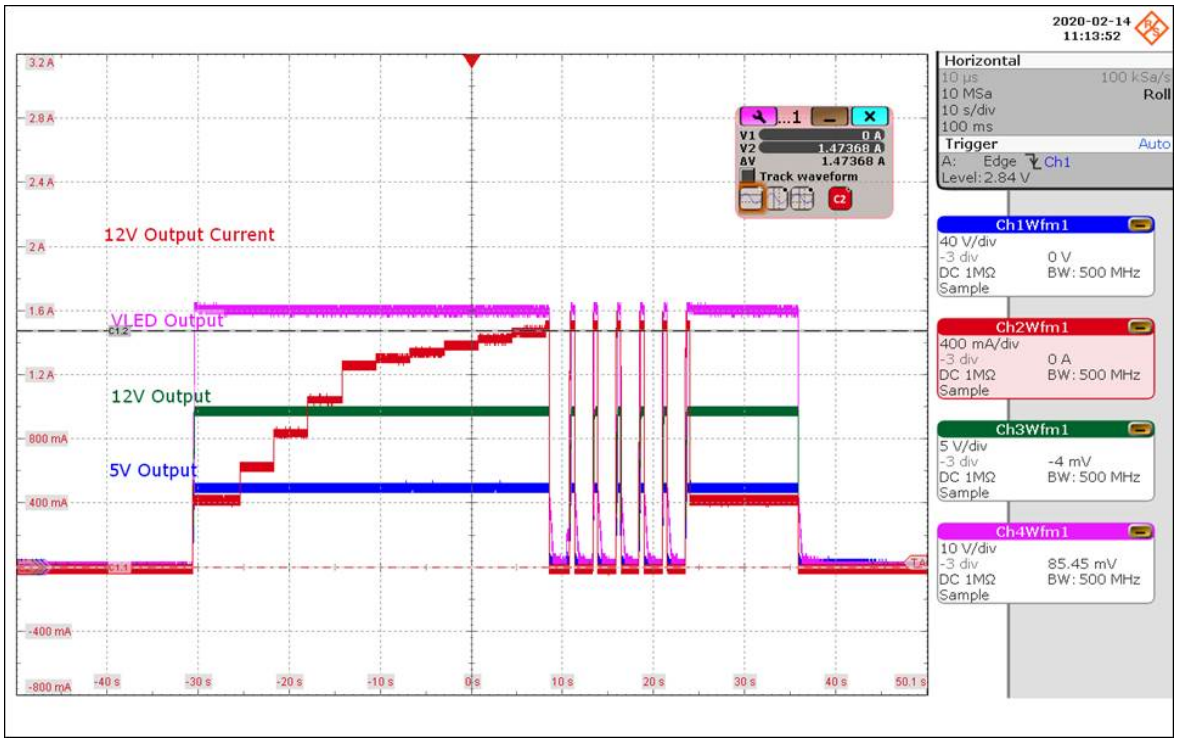

Figure 54 – CV2 Output Power Limit Test (WC) at 265 VAC.

10.12.3 LED Output Power Limit

The LED output power limit was tested by adding an external E-load in parallel with the LED string. Tests were carried out at line voltage 90 V and 265 V, with LED stack voltages 33 V, 37 V and 40 V. The test results are presented in the table below. The worst case output current thresholds measured were 0.748 A and 1.1 A accordingly. These tests are illustrated in Figure 55 and Figure 56 below.

V_{IN} [V_{RMS}]	I_{IN} [mA_{RMS}]	P_{IN} [W]	V_CV1 [V_{DC}]	I_CV1 [A_{DC}]	P_CV1 [W]	V_CV2 [V_{DC}]	I_CV2 [A_{DC}]	P_CV2 [W]	V_LED [V_{DC}]	P_LED [W]	LED Current Trip Point [mA]	P_{OUT} [W]
90	778	41.9	11.9	0.42	4.98	4.98	1	4.98	33.4	25.2	748.2	35.2
265	451	53.3	11.9	0.42	5.00	4.99	1	4.99	33.4	37.0	1103.8	47.0
90	794	43.1	11.9	0.42	4.99	4.99	1	4.98	37.2	26.1	706.5	36.1
265	452	53.3	11.9	0.42	5.01	5	1	5.00	37.1	37.2	1006.4	47.2
90	757	40.9	11.9	0.42	4.98	4.98	1	4.98	40.5	24.4	607.4	34.4
265	447	52.7	11.9	0.42	5.00	5	1	5.00	40.4	36.6	910.6	46.6

Table 11 – V_LED Output Power Limit.

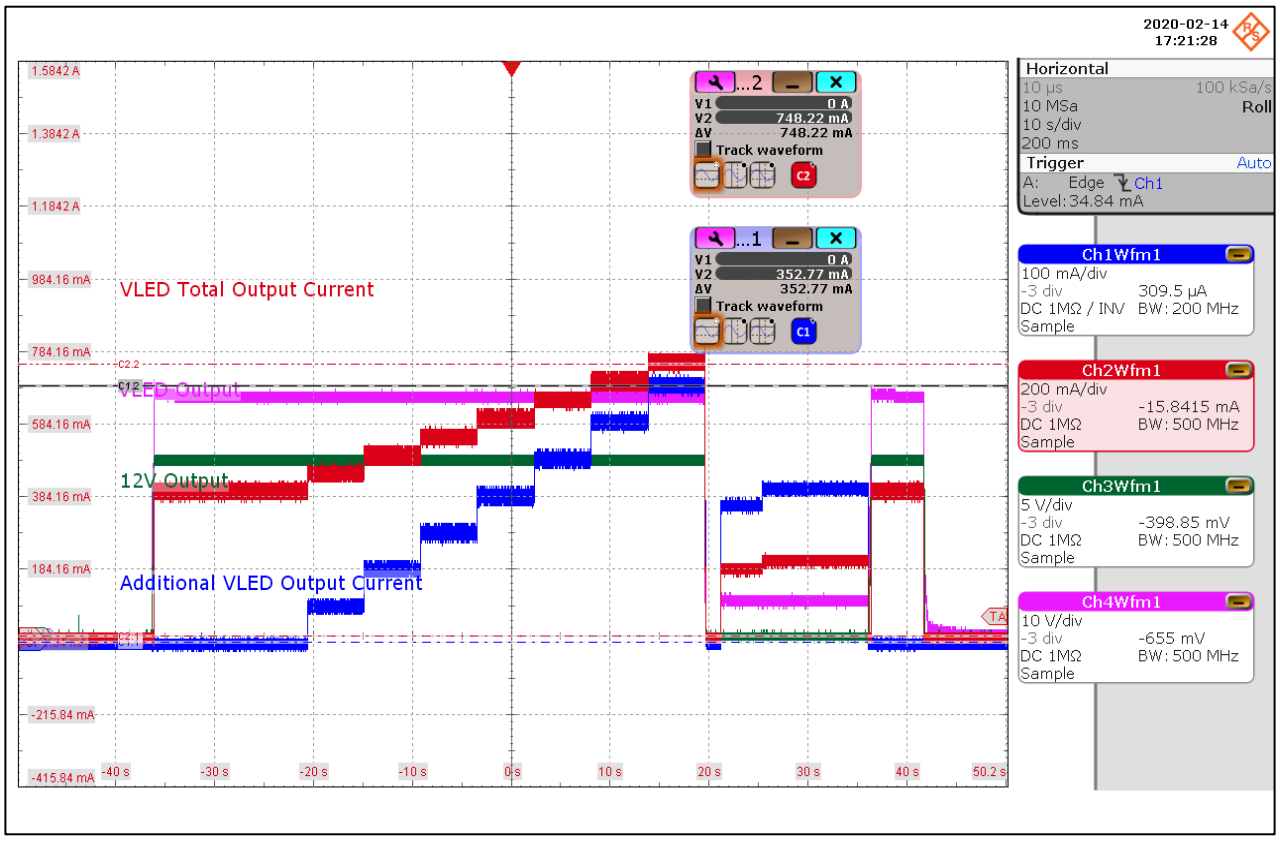

Figure 55 – LED Output Power Limit (WC) at 90 V Line.

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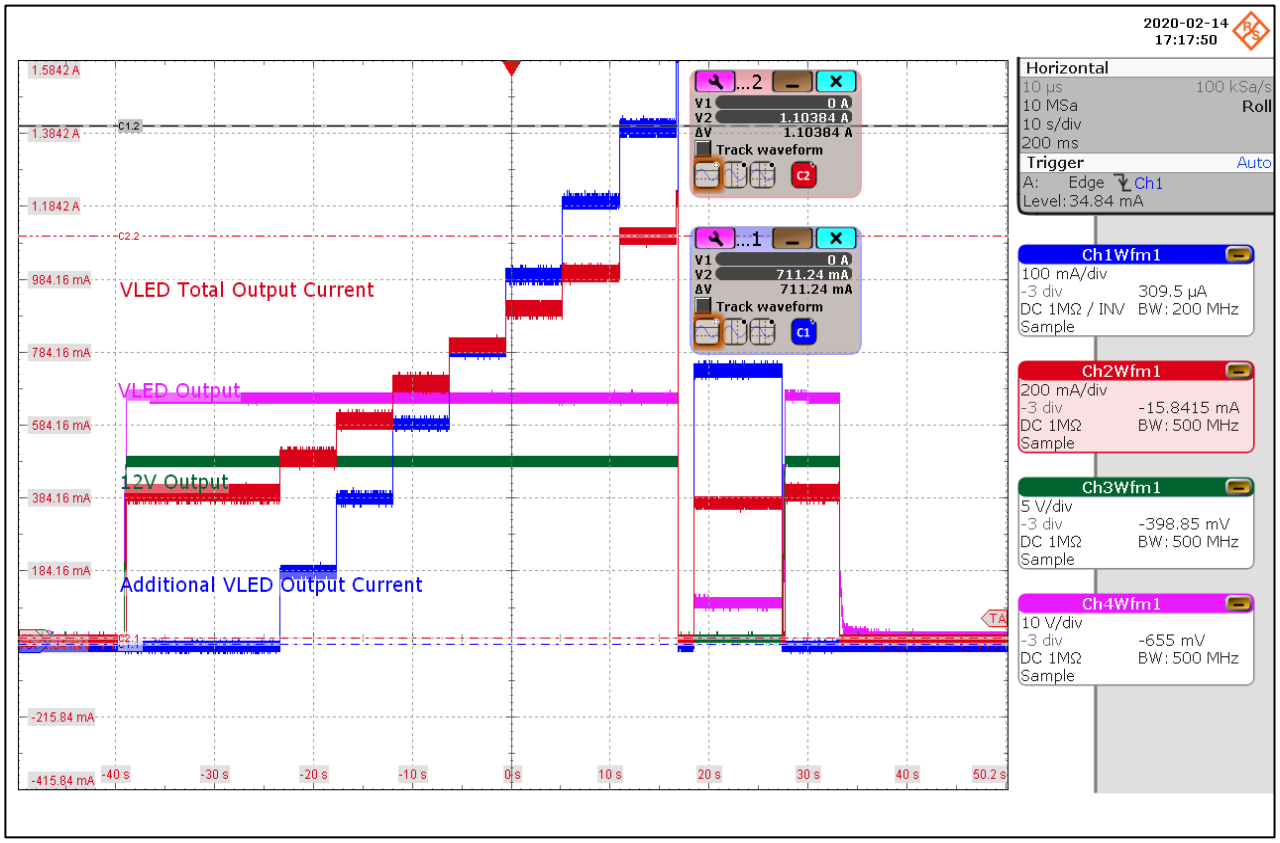

Figure 56 – LED Output Power Limit (WC) at 265 V Line.

10.12.4 CV1 and CV2 Output Overvoltage Protection

The overvoltage protection thresholds of the CV1 and CV2 outputs were tested at full power on all outputs. Additional charge was injected into the output filter capacitor of the output under test until the converter went into a restart. The test was carried out at line voltages 90 V and 265 V with 40 V LED stack voltage. The results are shown in the table below.

V_{IN} [V_{RMS}]	CV1 OVP [V_{DC}]	CV2 OVP [V_{DC}]	I_CV1 [A_{DC}]	I_CV2 [A_{DC}]
90	5.14	-	1	0.42
265	5.56	-	1	0.42
90	-	12.14	1	0.42
265	-	13.35	1	0.42

Table 12 – CV Outputs OVP Test.

10.12.5 LED Output Overvoltage Protection

The overvoltage protection thresholds of the LED output was tested at full power on all outputs. Additional charge was injected into the output filter capacitor of the LED output until the converter went into a restart. The test was carried out at line voltages 90 V and 265 V with 40 V LED stack voltage. The results are shown in the table below. Tests are further illustrated in Figure 57 and Figure 58.

V_{IN} [V_{RMS}]	I_{IN} [mA_{RMS}]	P_{IN} [W]	V_CV1 [V_{DC}]	I_CV1 [A_{DC}]	P_CV1 [W]	V_CV2 [V_{DC}]	I_CV2 [A_{DC}]	V_LED OVP [V_{DC}]	I_LED [mA]
90	0.611	32.2	5.02	1	5.0136	11.82	0.42	43.67	411.82
265	0.293	32.4	5.03	1	5.0296	11.93	0.42	47.01	405.49

Table 13 – LED Output OVP Test.

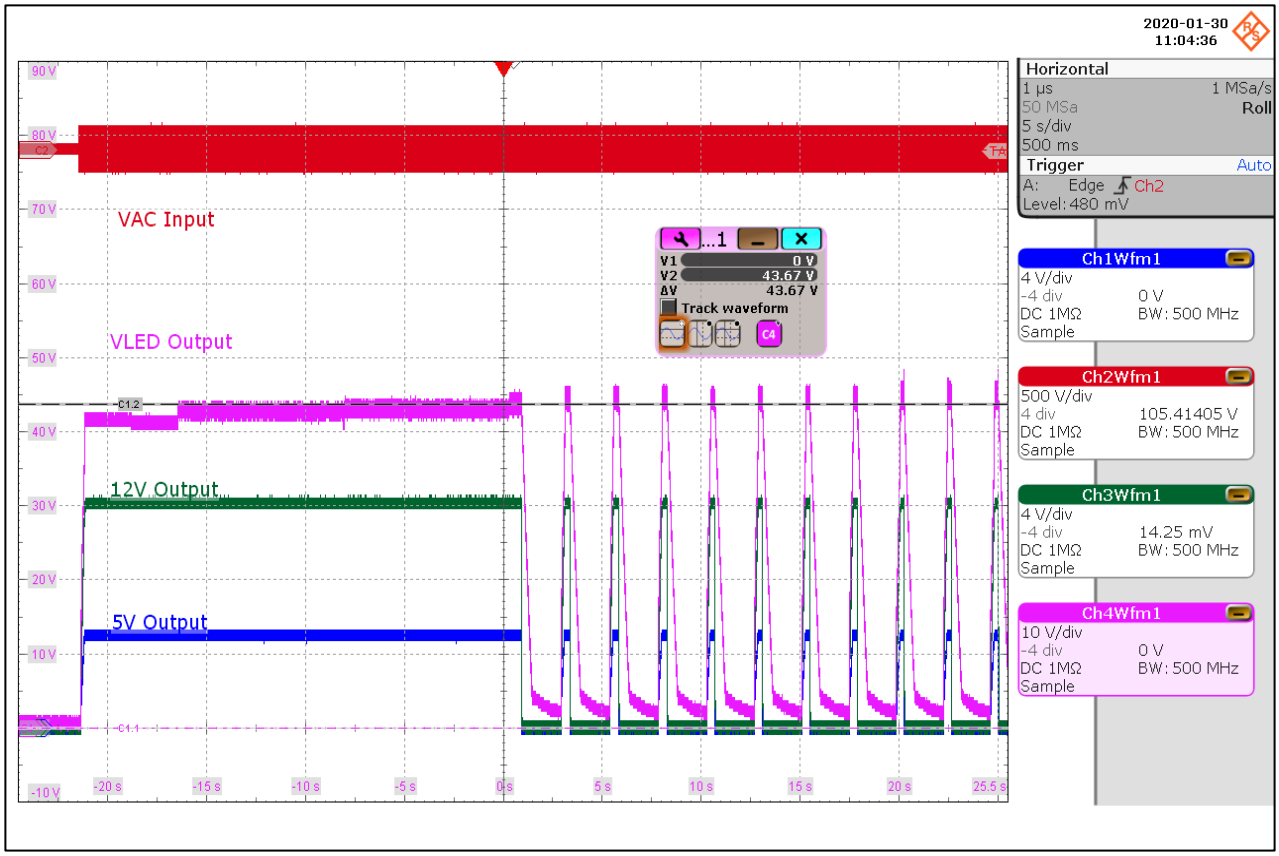

Figure 57 – LED Output OVP at Line Voltage 90 V.

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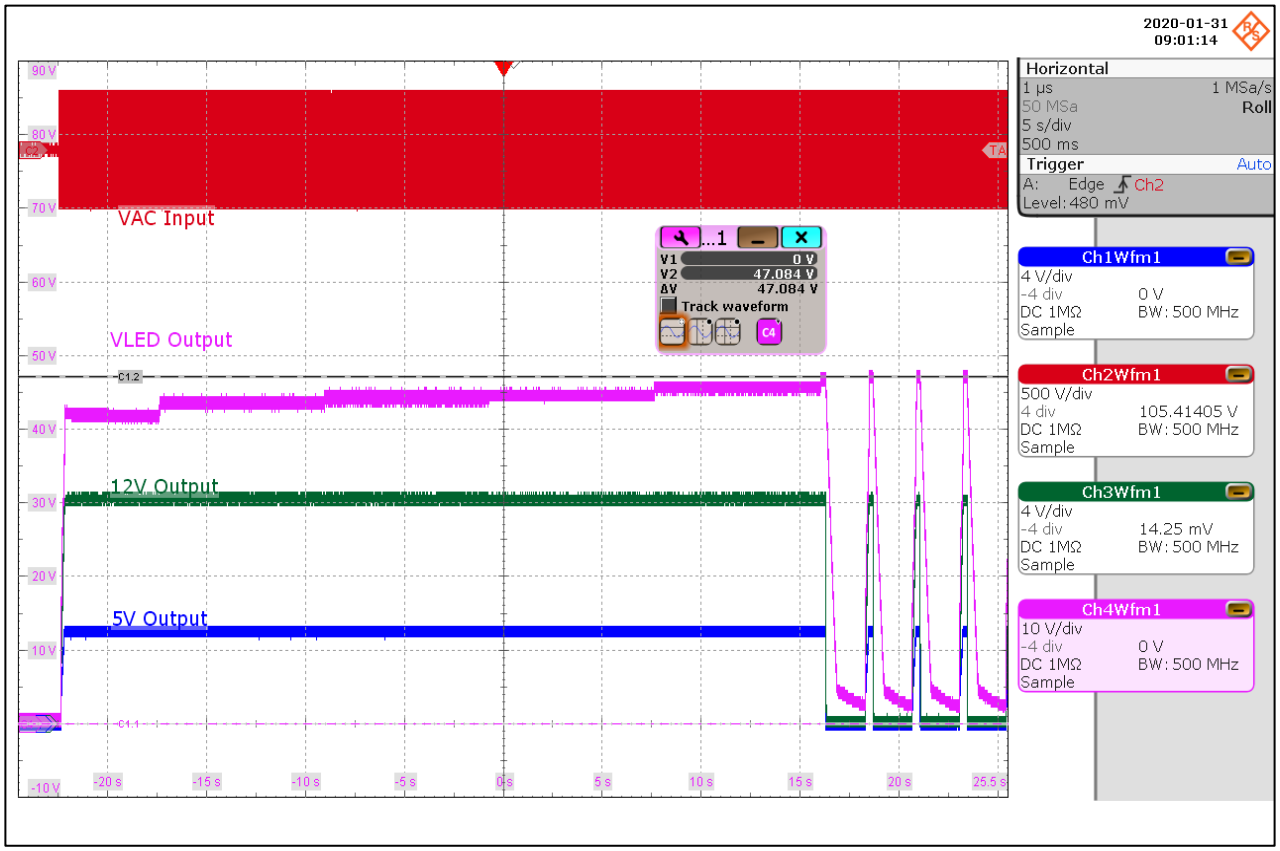

Figure 58 – LED Output OVP at Line Voltage 265 V.

10.13 *Output Ripple Measurements*

10.13.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe were utilized in order to reduce noise pick-up. Details of the probe modification are provided in Figure 59.

The probe adapter is shown in Figure 59. It includes a coaxial cable with two parallel capacitors connected to the points of measurement. The capacitors include a 0.1 μF / 100 V ceramic type and a 10 μF / 50 V aluminum electrolytic type. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be ensured.

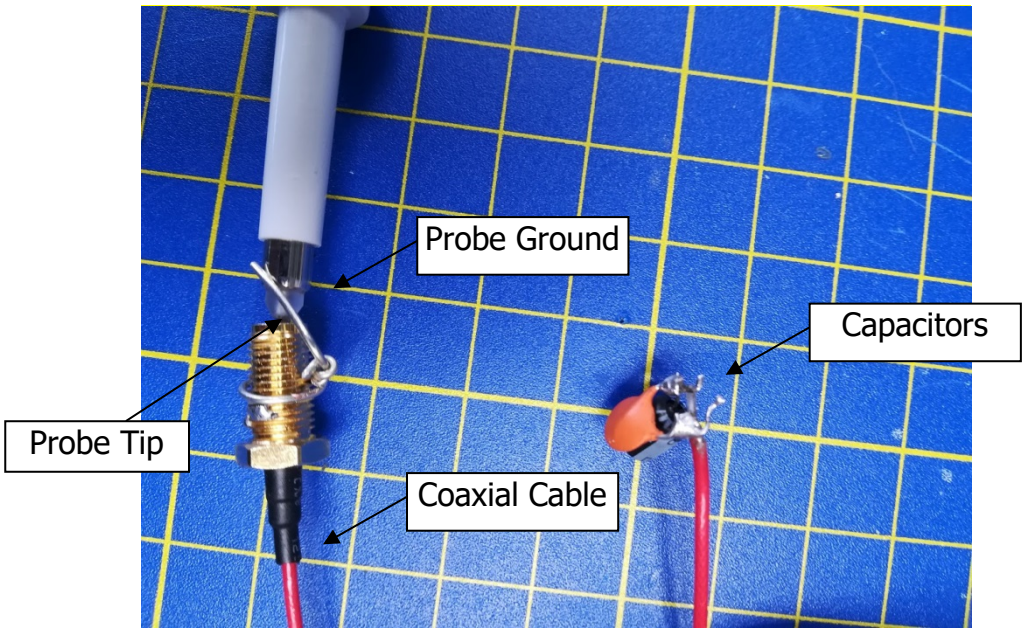

Figure 59 – Oscilloscope Probe Used in Ripple Measurement.

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10.13.2 CV1 Output Ripple

10.13.2.1 Test Set-up

- 90 VAC – 265 VAC
- Output 5 V @ 5 W, 12 V @ 15 W and LED_40 V @ 25 W
- 20 MHz bandwidth in the scope, 100 nF ceramic capacitor and 10 μF @ 50 V electrolytic capacitor with sniffing connected to output pin

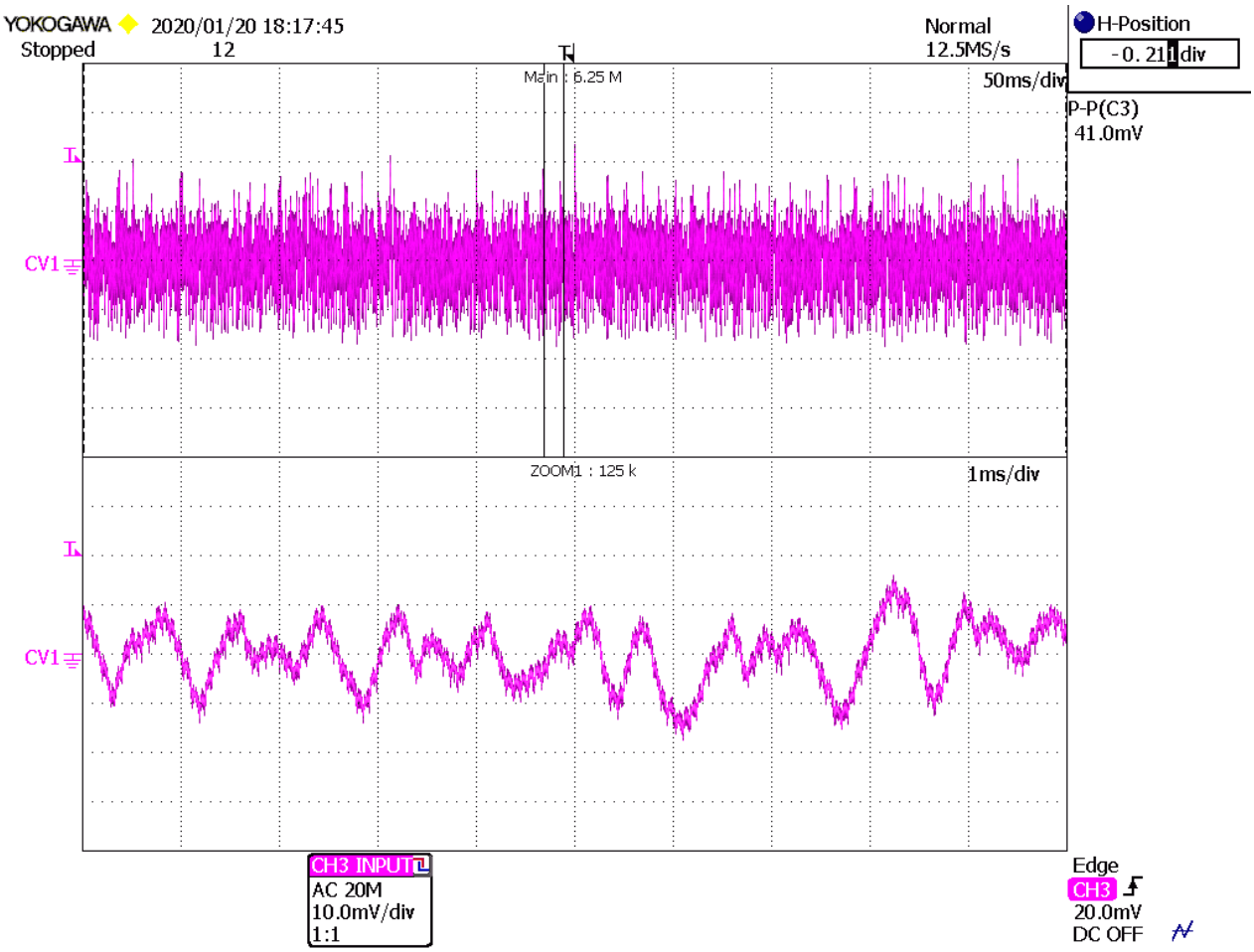

Figure 60 – VCV1 Ripple and Noise.

The worst case ripple and noise at the CV1 output of the converter was measured as 41 mV_{P-P}.

10.13.3 CV2 Output Ripple

10.13.3.1 Test Set-up

- 90 VAC – 265 VAC
- Output 5 V @ 5 W, 12 V @ 15 W and LED_40 V @ 25 W
- 20 MHz bandwidth in the scope, 100 nF ceramic capacitor

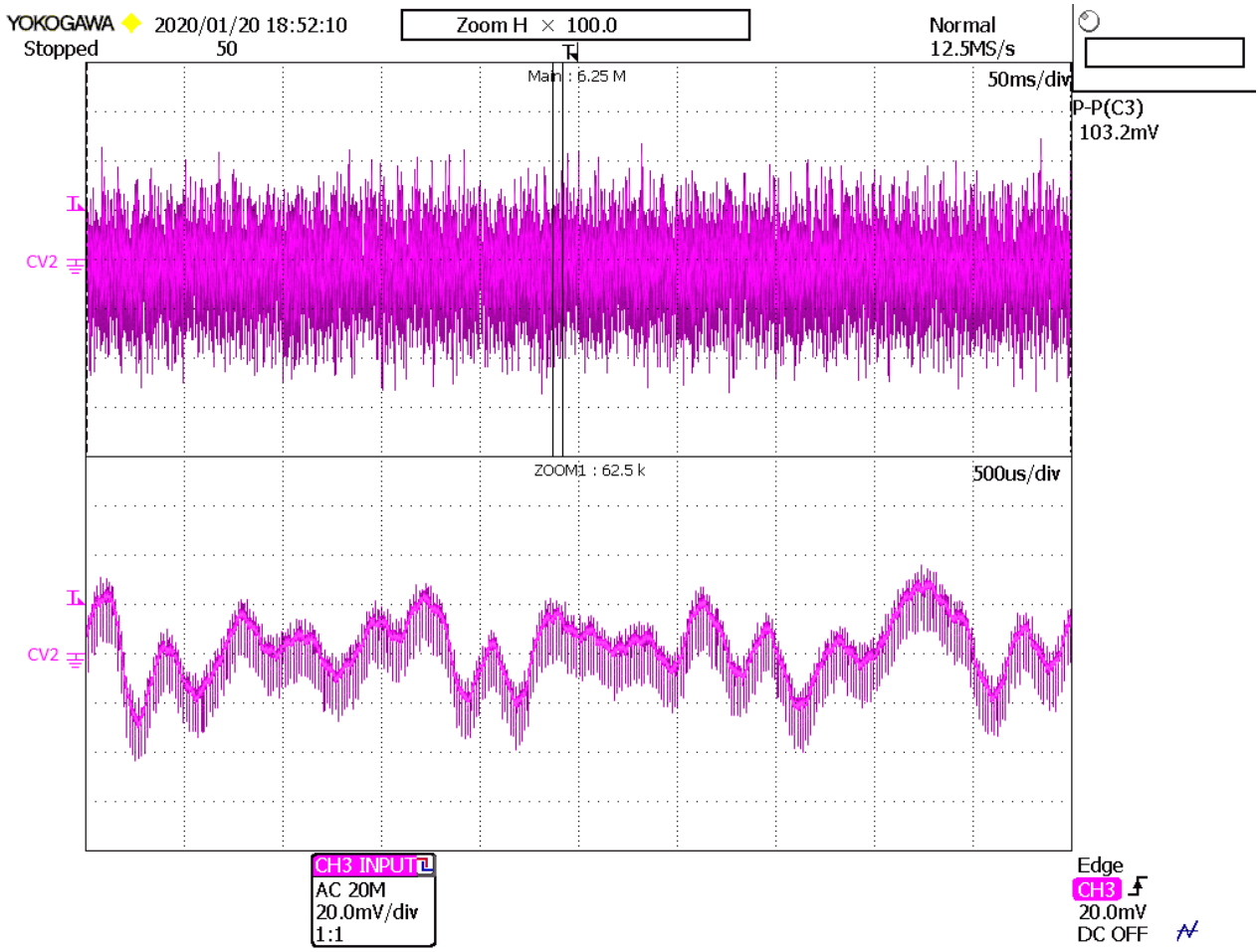

Figure 61 – Vo2 Ripple Waveform.

The worst case ripple and noise at the CV2 output of the converter was measured as 103.2 mV_{P-P}.

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10.14 *Conducted EMI*

The EMI scans were carried out at full power, with the secondary GND connected to EARTH. Note that the negative terminals of all main outputs (CV1, CV2 and LED) are connected to the same (secondary) GND. With worst-case test results, there is still 9.2 dB minimum margin.

In all cases, the conducted emissions were more than 10 dB below the limits set by CISPR22B / EN55022B.

10.14.1 Line Input 115 VAC

Voltage with 2-Line-LISN

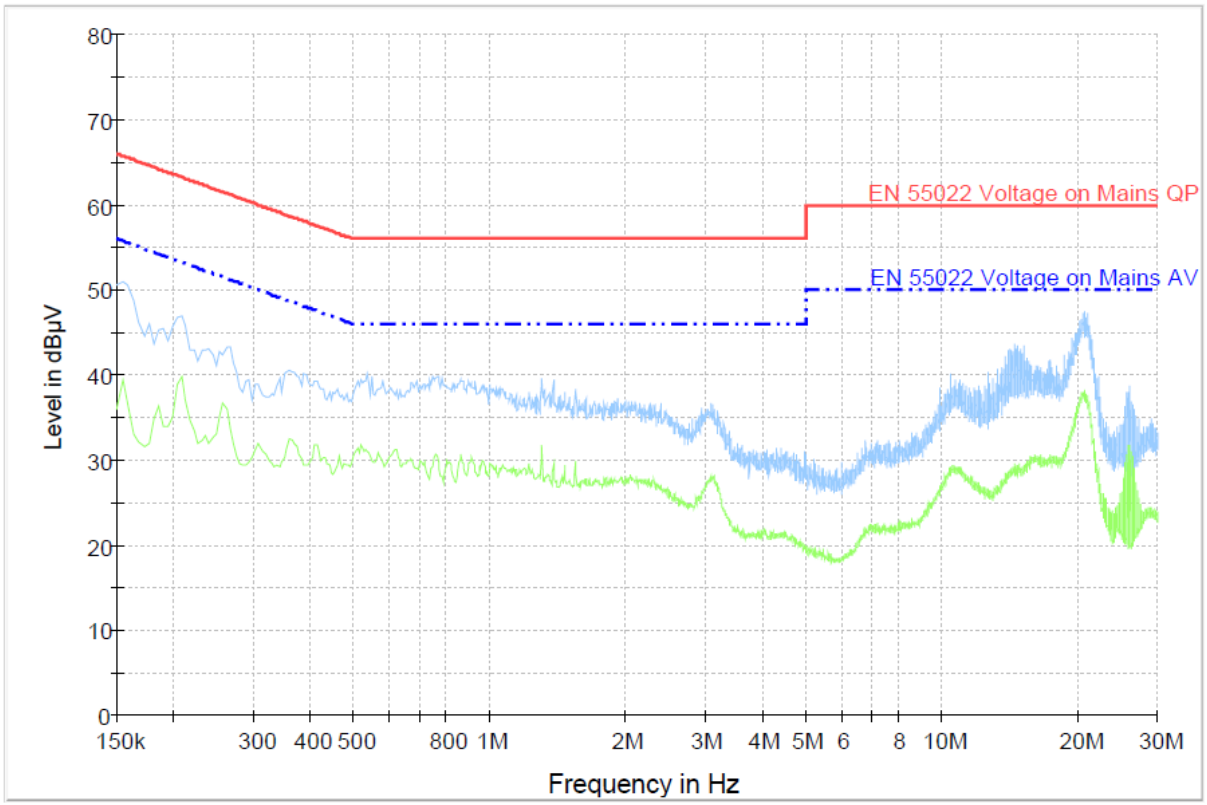

Figure 62 – EMI Test Results at 115 V.

10.14.2 Line Input 230 VAC

Voltage with 2-Line-LISN

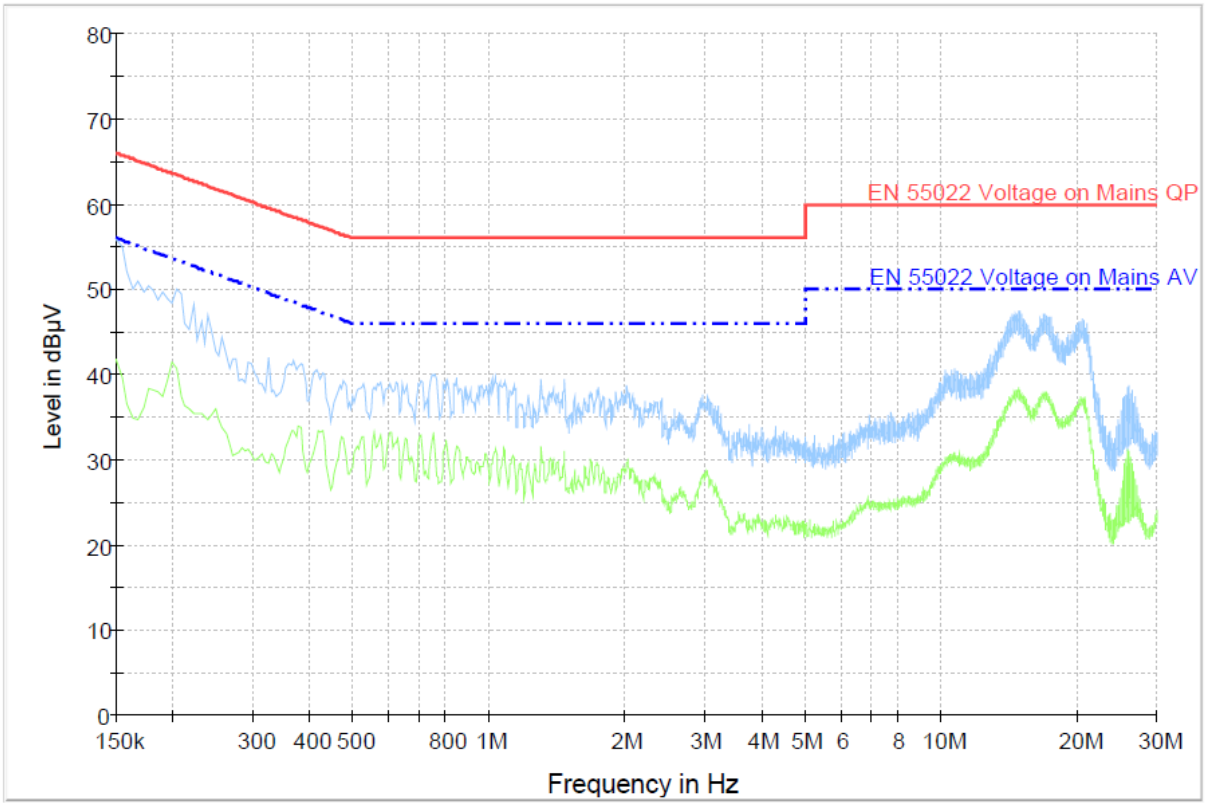

Figure 63 – EMI Test Results at 230 V.

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10.15 *Thermal Performance*

There are no heat sinks in cooling arrangements of the assembly. Copper pours are used for the cooling of the two control ICs. No forced air-cooling was deployed during test. The temperatures of the hottest components in the assembly are shown in Table 14.

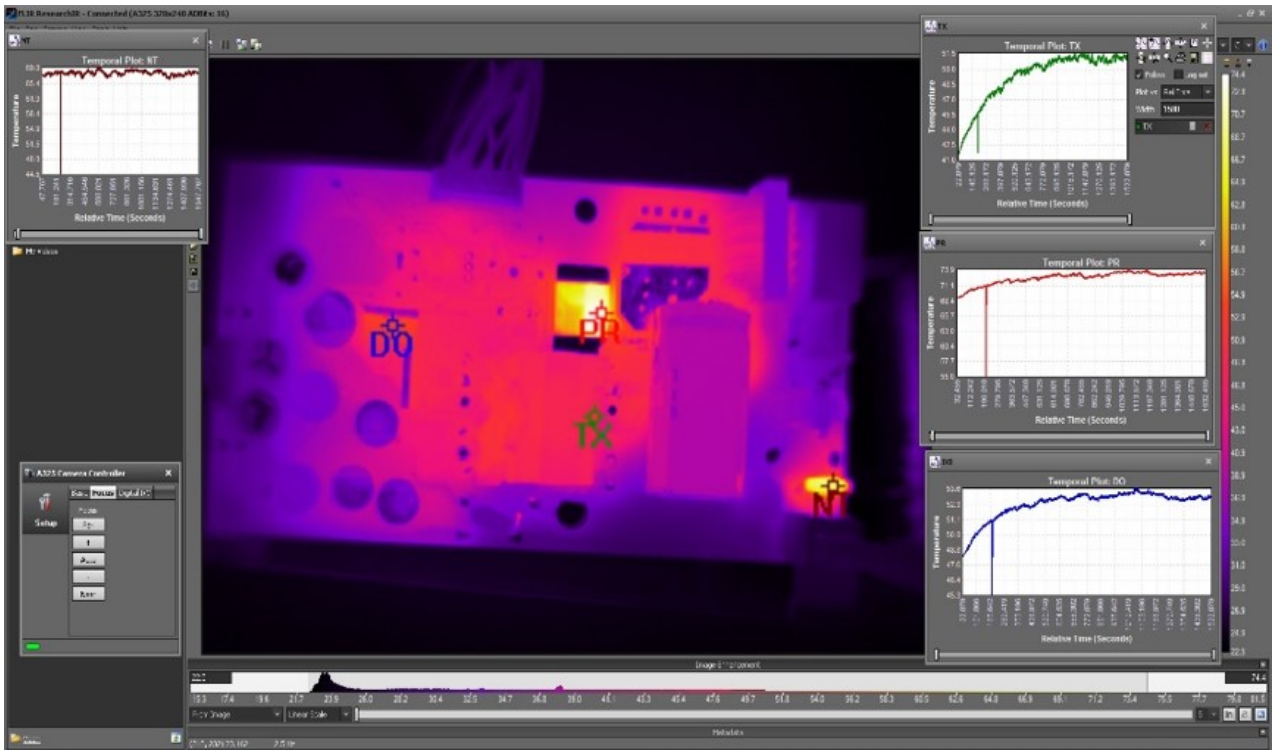

Figure 64 – Line = 90 V Full Power - Thermal Image - Top View.

Part	U2 Inno-PS	D3 LED Diode	R12 NTC	T1 Transformer
T [ºC]	74	54	67	52
ΔT [ºC]	52	32	45	30

Table 14 – Line = 90 V Full Power – Component Temperatures

11 Revision History

Date	Author	Revision	Description & Changes	Reviewed
17-Apr-20	AL	1.0	Initial Release.	Apps & Mktg

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