Application Note AN-89
InnoMux PSU Family

InnoMux PSU Tips, Techniques and Troubleshooting Guide

This Application Note (AN) should be read in conjunction with and in the context of the PI InnoSwitch™3-MX and InnoMux™ Family data sheets:

https://ac-dc.power.com/sites/default/files/product_document/data_sheet/InnoSwitch3-MX-data-sheet.pdf

https://ac-dc.power.com/sites/default/files/product_document/data_sheet/InnoMux-data-sheet.pdf

Applications Example

The circuit shown in Figure 1 describes a typical converter comprising two CV outputs and a single CC (LED) output, suitable for a range of television applications. This single-stage, multiple-output, flyback architecture enables high efficiency across the universal line range, easily complying with the latest ENERGY STAR® standards. The high-accuracy CV outputs are independently regulated and have very fast load transient response. The CC output is configurable for a variety of dimming modes, including analogue dimming, straight PWM dimming, filtered PWM dimming, and hybrid dimming.

For a comprehensive design example report, please refer to DER-635: 45 W Multi-output Flyback Converter with Two CV and One CC using InnoMux IMX111U and InnoSwitch3-MX INN3468C.

https://ac-dc.power.com/der-635

Key Application Considerations

Output Power Table

The Output Power Table on page 1 of the InnoSwitch3-MX family data sheet represents the maximum practical continuous output power level that can be obtained under the following conditions:

A. The minimum DC input voltage is 90 V or higher for 85 VAC. An input capacitor with appropriate voltage and ripple current rating should be chosen.
B. Efficiency assumptions depend on power level and the application type. In computer monitor applications, a minimum efficiency of 85.5% should be the target in order to meet ENERGY STAR Displays Version 8.0 requirements.
C. A default maximum ambient temperature of 50 °C is assumed.

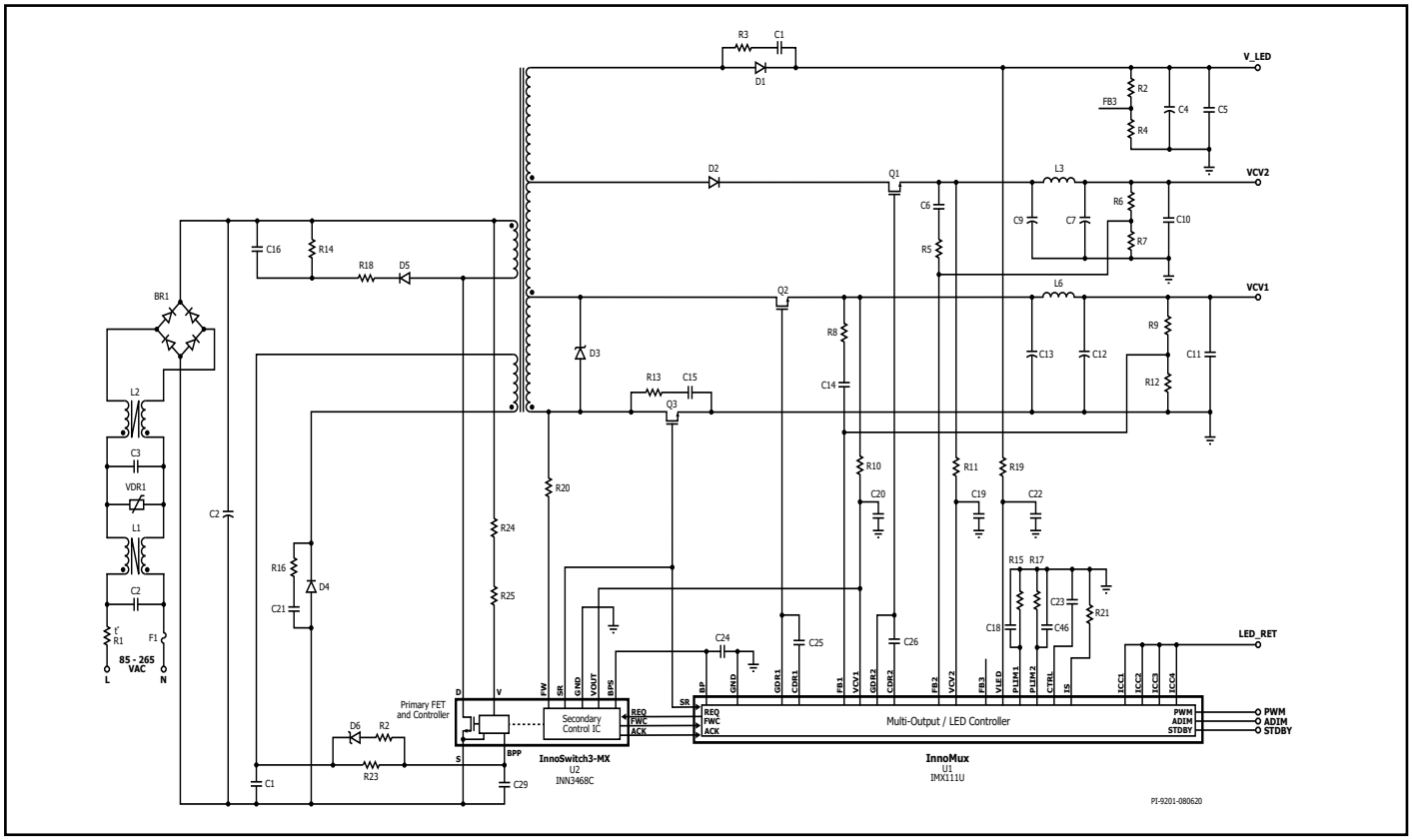

Figure 1. Applications Example Schematic (2 × CV Outputs + 1 × CC (LED) Output).

InnoSwitch3-MX Primary Auxiliary (BYPASS) Supply

By default, the primary circuitry of the InnoSwitch3-MX is powered internally from the DRAIN (D) pin via the PRIMARY BYPASS (BPP) pin regulator. A PRIMARY BYPASS (BPP) pin filter capacitor (C29 in Figure 1) should be connected between the PRIMARY BYPASS (BPP) pin and the SOURCE (S) pin of the device with the shortest connections possible. To reduce the power dissipation in the PRIMARY BYPASS (BPP) pin regulator, an auxiliary (bypass) winding may be added to the main transformer. The voltage from this winding is rectified and connected to the PRIMARY BYPASS (BPP) pin capacitor via an appropriate size resistor (R14 in Figure 1). The value of R14 should be adjusted to achieve the lowest no-load input power. The capacitance of the PRIMARY BYPASS (BPP) pin capacitor is also used to select the primary current limit (I_{LIM}). A 0.47 nF capacitor selects STANDARD current limit, and a 4.7 µF capacitor selects INCREASED as shown in the respective tables on pages 9 and 10 of the InnoSwitch3-MX data sheets. Though the use of aluminium electrolytic capacitors is not precluded, multilayer ceramic capacitors are preferred, because they can be placed closer to the device pins. A 16 V or 25 V rated X5R or X7R dielectric capacitors are recommended.

Primary Bias Winding and External Bias Circuit

The turns ratio for the bias winding should be selected such that 7 V is developed across C1 (Figure 1) in STANDBY mode. The bias current from the external circuit should be set to approximately 30 mA to achieve lowest no-load power consumption, when operating the power supply at 230 VAC input, (V_{BPP} > 5 V). A glass passivated standard recovery rectifier diode with low junction capacitance is recommended to avoid the snappy recovery typically seen with fast or ultrafast diodes that can lead to higher radiated EMI. An aluminium capacitor (C1) of at least 22 µF with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended. Typically, the highest voltage across C1 is developed when the converter is operated at full power and at the lowest line voltage.

InnoMux Controller Supply

In steady-state, the controller is supplied from the OUTPUT VOLTAGE (CV2) pin provided that the voltage on the OUTPUT VOLTAGE (CV2) pin is V_{CV2} >$V_{CV2(MIN)}$. An internal voltage regulator reduces the voltage on the OUTPUT VOLTAGE (CV2) pin to a 5 V rail, which powers the internal circuitry of the controller. The 5 V output of the internal regulator is available on the BYPASS (BP) pin and is typically used to supply the secondary circuitry SECONDARY BYPASS (BPS) pin of the InnoSwitch3-MX controller in the chip set. Good quality ceramic capacitors should be used as local de-couplers at the InnoMux BYPASS (BP) pin and at the InnoSwitch3-MX SECONDARY BYPASS (BPS) pin to GROUND (GND) pin. The connections between these capacitors to the actual IC pins and to GROUND (GND) pin should be very short. In single CV output applications, the OUTPUT VOLTAGE (CV1) pin should be connected to the OUTPUT VOLTAGE (CV2) pin of the controller.

If V_{CV2} <$V_{CV2(MIN)}$, the controller is supplied from the voltage at the OUTPUT VOLTAGE (VLED) pin. To avoid excessive dissipation in the internal regulator, an unregulated secondary auxiliary winding L_{AUX} (Figure 2) can be added to the transformer to power the OUTPUT VOLTAGE (VC2) pin. The same rationale applies if a second CV output is present but V_{CV2} >>$V_{CV2(MIN}$. To avoid using heavy gauge wire it is most appropriate for the auxiliary winding to remain outside the stack of the main outputs' secondary windings. Figure 2 illustrates a case where the auxiliary winding is referenced to the "top" of the CV1 secondary. Since V_{CV1} = 5 V, W_{AUX} is made of very small number of turns (2-3) of a small diameter wire and takes very little of the bobbin window. At light load, the rectified voltage from this winding must be above $V_{CV2(MIN)}$. At full load, the voltage on the OUTPUT VOLTAGE (CV2) pin should be about 8 V (30 mA consumption).

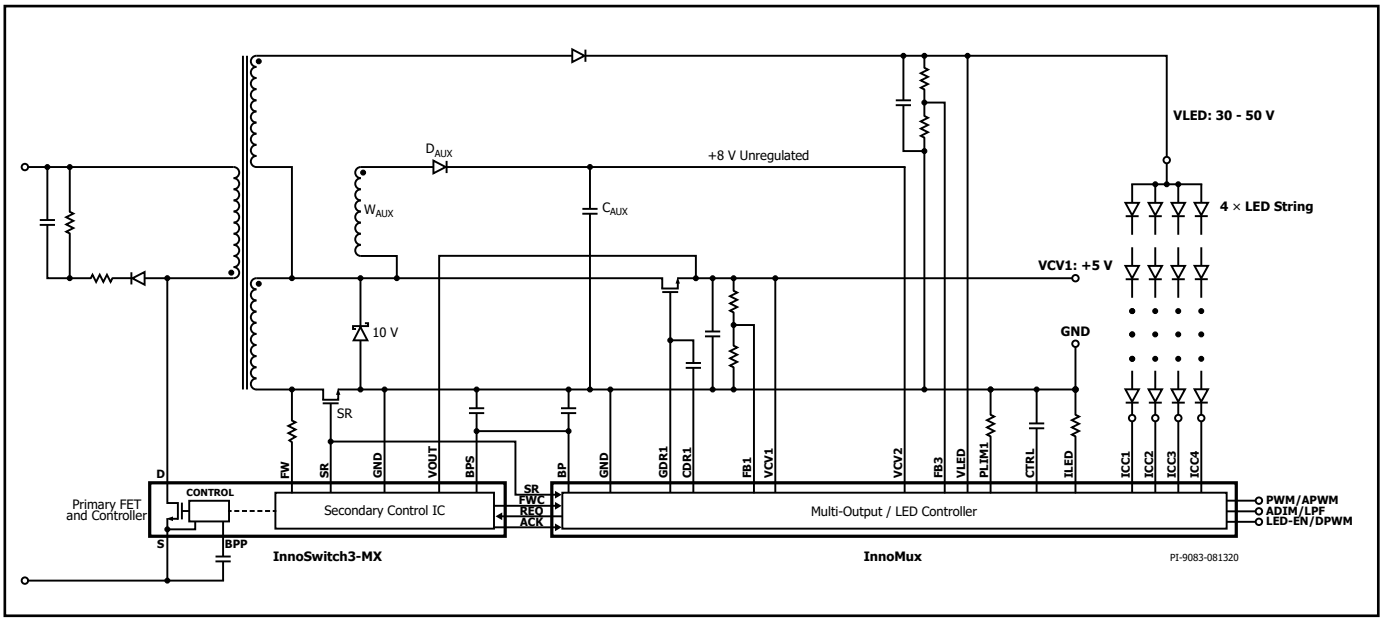

Figure 2. An Unregulated 8 V Auxiliary Supply (W_{AUX}, D_{AUX} and C_{AUX}) Reducing the Internal Dissipation in InnoMux.

An alternative circuit providing supply for the InnoMux controller is shown in Figure 3. There the CV2 regulator of the controller is used with a low power selection FET (Q2) and a diode (D2) to provide power to InnoMux. Since the power consumption of the controller is generally low, low-cost devices (D2 and Q2) may be used. High R_{DSON} Q2 may result in significant voltage drop across its channel at the beginning of the secondary conduction interval. This will need to be taken into account when calculating the transformer turns ratio. To avoid overspill completely the following relation must be true:

$$(V_F + R_{DS(ON)} \times I_{CV(PK)} + V_{CV2}) \frac{N_{CV} + N_{CC}}{N_{CV}} < V_F + V_{LED}$$ Equation 1a

There VF is the diode forward voltage; $R_{DS(ON)}$ is the Q2 channel resistance; VCV2 is the required supply voltage to the OUTPUT VOLTAGE (VCV2) pin (8 V typical); VLED is the minimum LED string voltage; NCV and NCC are the number of secondary turns in the transformer as indicated in Figure 3. Some degree of overspill is tolerable since the request frequency of the CV2 channel is very low.

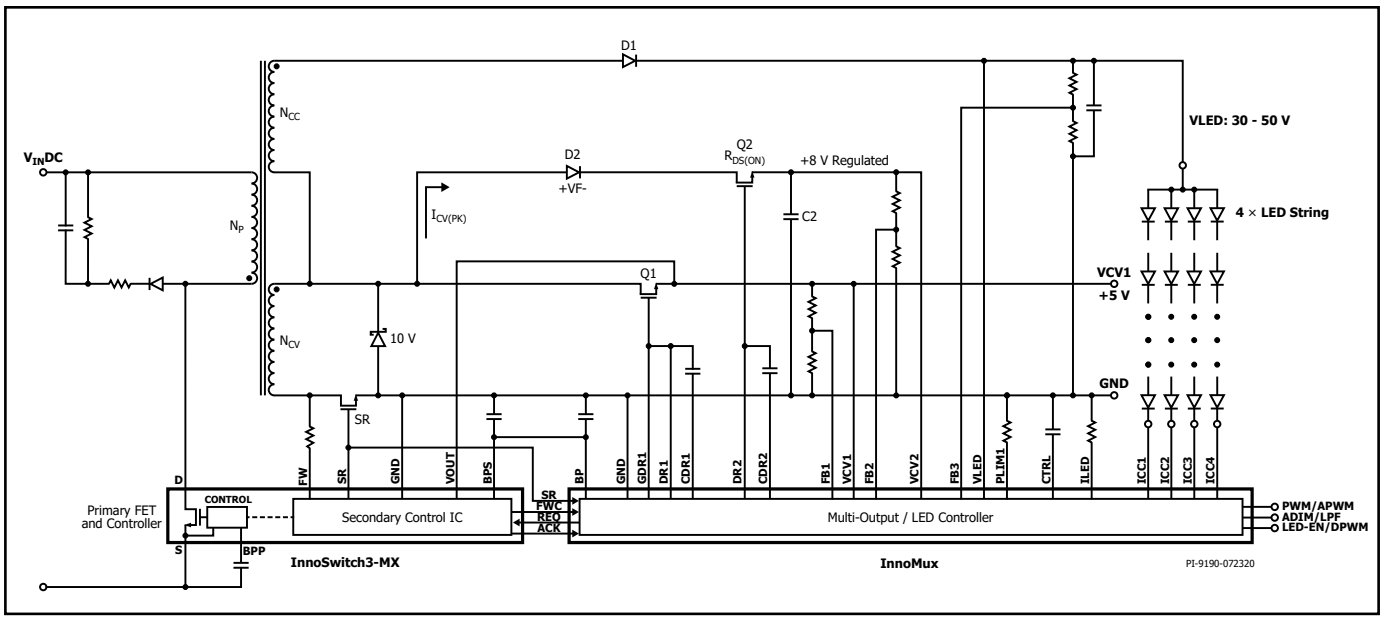

Figure 3. A Regulated 8 V Auxiliary Supply (D2, Q2) Supplying Power to InnoMux.

Primary-Side Overvoltage Protection

The InnoSwitch3-MX primary-side output overvoltage protection uses an internal latch, triggered when the current into the PRIMARY BYPASS (BPP) pin exceeds a certain threshold, I_{SD}. A crude primary-sensed, output OVP function can be constructed by connecting a series combination of a Zener diode (D8), a resistor (R37), and a blocking diode in parallel with R14. It should be verified experimentally that the OVP is not triggered when the converter is operated on full power at the lowest line voltage.

Line UV and OV Protection

Resistors connected from the UNDER/OVER INPUT VOLTAGE (V) pin to the DC bus enable sensing of input voltage to provide line undervoltage and overvoltage protection. For a typical universal input application, a resistor value of 3.8 MΩ is recommended.

Figure 4 shows circuit configurations that enable either the line UV or the line OV feature only to be enabled. InnoSwitch3-MX features a primary-sensed OV protection feature that can be used to latch-off the power supply. Once the power supply is latched off, it can be reset, if the UNDER/OVER INPUT VOLTAGE (V) pin current is reduced to zero. Once the power supply is latched off, even after the input supply is turned off, it can take considerable time to reset the InnoSwitch3-MX controller, as the energy stored in the input capacitor will continue to provide current to the controller.

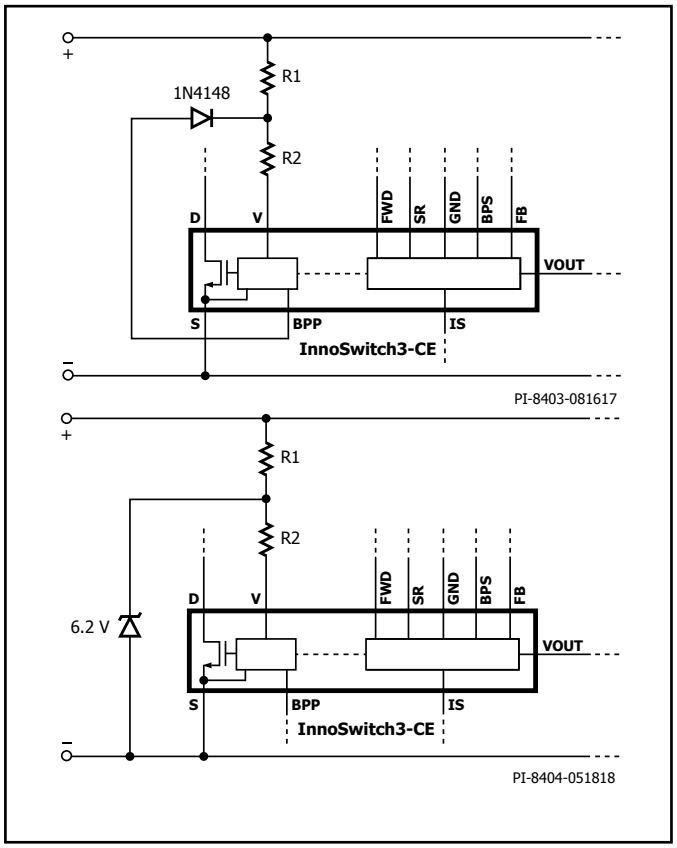

Figure 4. Above – Line OVP Only; Below – Line UVP Only.

A fast AC reset can be achieved using the modified circuit configuration shown in Figure 5. The voltage across capacitor C_S reduces rapidly after the input supply is disconnected, reducing current into the UNDER/OVER INPUT VOLTAGE (V) pin.

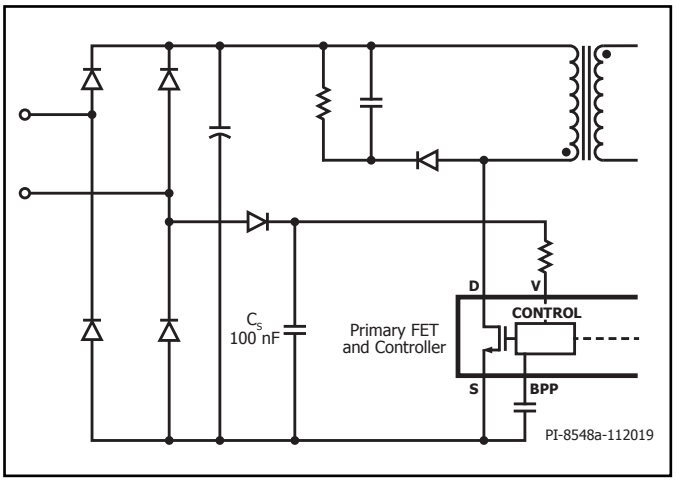

Figure 5. Fast Reset Circuit.

Component Selection

Primary-Side Snubber

A snubber circuit (D9, R1, R2, C18) should be used on the primary-side as shown in Figure 1. This prevents excess voltage spikes at the drain of the primary switch at the instant of turn-off of the MOSFET during each switching cycle, though conventional RCD clamps can be used. Resistor R1 in series with the clamp diode D9 dampens the ringing at the drain and also limits the reverse current through the clamp diode during reverse recovery. Standard recovery glass passivated diodes with low junction capacitance are recommended as these enable partial energy recovery from the clamp thereby improving efficiency.

Transformer Considerations

The transformer could have independent secondary windings (Figure 1) or stacked windings (Figure 2) or any combination of the two. For the correct operation of the topology, it is essential that the turns ratios of the main outputs' secondary windings are chosen such that:

$$\frac{V_{CV1}}{N_{CV1}} < \frac{V_{CV2}}{N_{CV2}} < \frac{V_{CC}}{N_{CC}} \qquad \text{Equation 1}$$

where V_{CV1}, V_{CV2}, and V_{CC} are the voltages across the CV1, CV2, and CC winding respectively, during the corresponding conduction intervals of these windings; N_{CV1}, N_{CV2}, N_{CC}, are the number of turns in the windings. Where the PSU is required to work with LED strings having a wide range of LED voltages, or intended for use with several different LED strings, V_{CC} is the minimum LED voltage in the range.

Selection FET Choice

The gate drive pulses to the selection FETs generated by InnoMux do not exceed 5 V. It is therefore essential that MOSFETs with low gate-drive threshold $V_{GS(TH)}$ are utilized. $V_{GS(TH)}$ < 3.5 V is recommended.

SR FET Selection

The synchronous rectifier MOSFET conducts the combined current in the return of the transformer. i.e. the combined current of all output rectifiers. A low $R_{DS(ON)}$ MOSFET should be utilized in order to reduce the conduction loss in the device. However, at the FORWARD (FW) pin, the voltage across the enhanced channel of the SR is compared

to a fixed internal threshold to determine the point at which the SR is gated OFF. Consequently, an SR with very low $R_{DS(ON)}$ will cause the channel to be depleted too early before the end of the secondary conduction interval, thus leaving the rest of the rectification to be completed through the SR body diode. This will increase the conduction loss in the SR. The described loss of synchronous rectification could be particularly acute with the CC winding since typically $N_{CV1} < N_{CV2} < N_{CC}$ as shown in Figure 6.

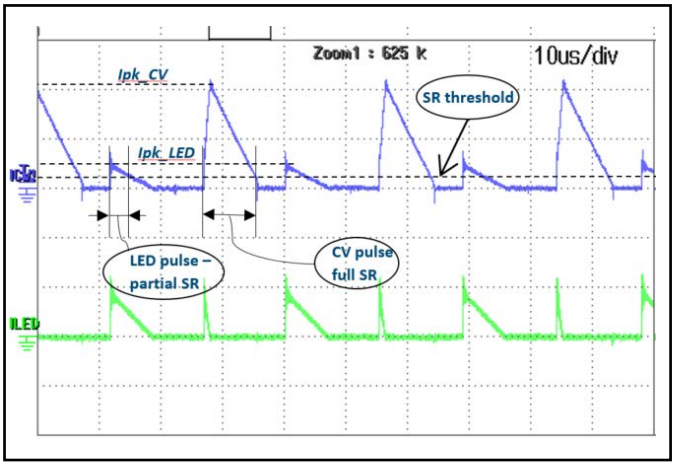

Figure 6. Typical SR and CC Winding Current Waveform.

The $V_{GS(TH)}$ threshold requirement of the SR FET is the same as that of the selection FETs.

Recommendations for Circuit Board Layout

The PCB layout recommendations concerning the InnoSwitch3-MX controller are very similar to those of the InnoSwitch3 family. Details can be found at https://ac-dc.power.com/products/innoswitch-family/innoswitch3-ce/. The primary switch in InnoSwitch3-MX IC is cooled through the SOURCE pin (the "paddle") of the IC. Care should be taken that the thermal impedance between the SOURCE pin and the cooling copper of the PCB is kept to a minimum. For best results, the cooling copper pour should flare out as rapidly as possible away from the solder joint. In the case of double sided PCB with cooling copper on both sides the multiple vias close to the paddle should be used to connect the copper on both sides.

The main difference between the InnoSwitch3 stand-alone controllers and the InnoSwitch3-MX controller as a part of the InnoMux chipset is the presence of communication pins (REQ, ACK, and FWC). These pins are connected to the identically named pins of the InnoMux controller forming the communication lines between the two controllers. These communication lines must be kept short, and where possible, screened from electromagnetic noise. Ideally, the connection between the GROUND (GND) pins of InnoSwitch3-MX and InnoMux should not be shared with any AC ripple current in the output filter stages, load currents or any other heavy currents closing to the secondary ground potential. This is important in order to achieve accurate synchronous rectification.

To minimize output ripple and avoid generating EMI, it is advisable to minimize the length of the connection between the negative terminals of all output filter capacitors to the source of the SR.

To minimize crosstalk between the outputs of the converter, the paths connecting the negative terminals of the output filter capacitors of each output to the SR source should be separate.

A 2xCV 1xLED (CC) converter PCB layout example is shown in Figure 7 below.

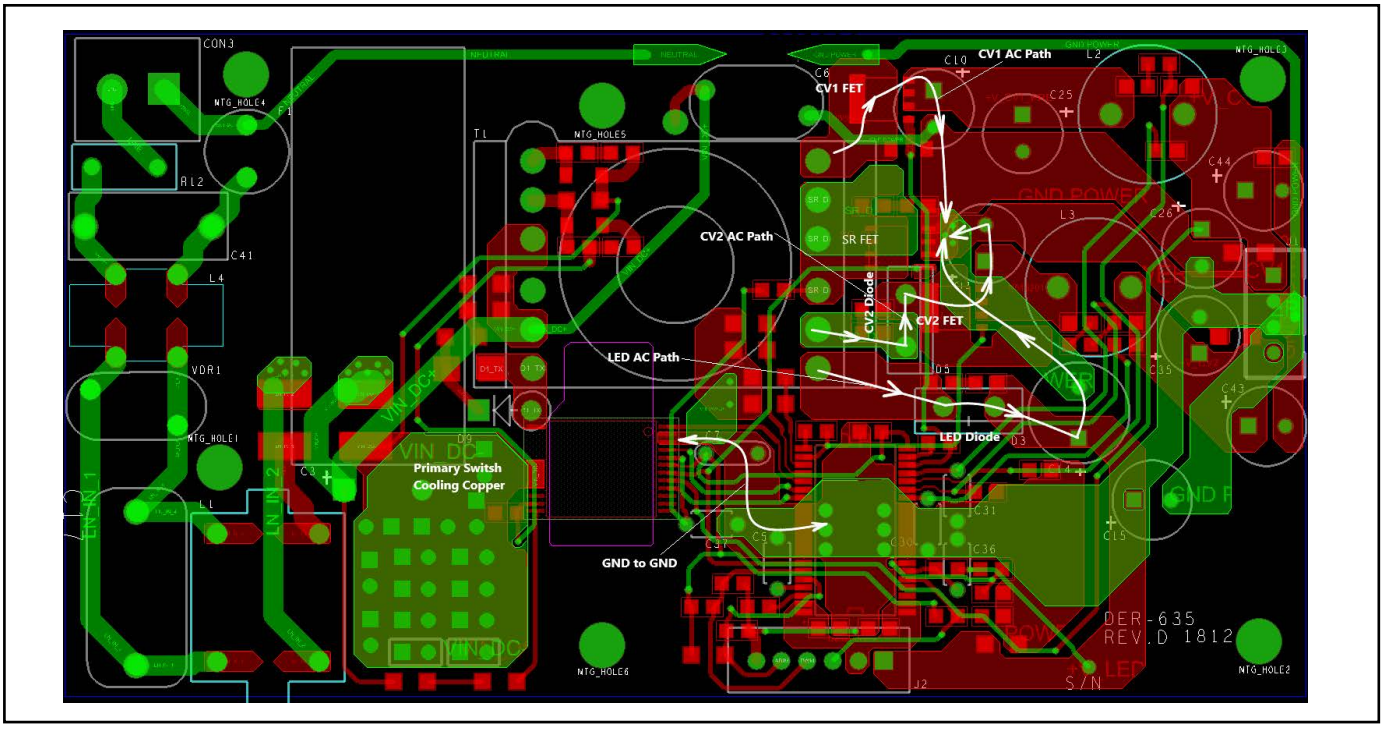

Figure 7. Two CV + 1 LED (CC) Output Converter – PCB Layout Example.

PI Expert Design Tool

In an InnoMux-controlled multiple-output flyback converter, output regulation is maintained by appropriately multiplexing the energy stored in the transformer among all participating outputs. Such control technique makes it difficult to use conventional flyback definitions and to follow the established design practice. In order to assist the user in the SMPS design with the InnoMux chipset, Power Integrations has made available a free on-line design tool:

https://piexpertonline.power.com/pixls/design/index

The design calculations implemented by the tool are based on the following assumptions and approximations:

1. It is assumed that at any one switching cycle, the primary of the converter delivers energy to only one of the main converter outputs.
2. It is further assumed that at any given switching cycle, the converter is in steady-state in the same way it would be if the entire output power were delivered continuously to this one output only. This allows a current continuity factor KP_N to be defined for each output during the time interval this output receives energy from the primary.
3. In another approximation, the rectified line voltage across the input filter capacitor is replaced by a DC voltage with the same average value.

Under assumptions 1) and 2), the power delivered to any output is controlled by the rate of occurrence (request frequency) and the length of the time interval during which that output receives energy from the primary of the transformer. On average this time interval may include one or more (not necessarily integer number of) primary switching cycles. Furthermore, if all outputs operate in BCM or DCM, the primary switching frequency f_S and the primary peak current I_P remain the same. For a particular output (n), a system Duty Cycle D_N can be formulated as follows:

$$D_N = PO_N / PO_{TOT} \qquad \text{Equation 2}$$

where PO_N is the power delivered to the output, and PO_{TOT} is the total power delivered to all outputs of the converter. Assumption 3) obviates the need for integrating any of the electrical quantities (currents, voltages, frequencies, current continuity factors etc.) over the mains cycle in order to obtain their long-term average or RMS values. For example, the RMS values of the current in a transformer secondary (n) could be calculated directly from the system duty-cycle D_N and the cycle RMS current $I_{RMS2CYCN}$ of the output as indicated by

$$I2RMS_n = \sqrt{D\_SYS_n} \times Irms2cyc_n \qquad \text{Equation 3}$$

The numerical values of the electrical quantities returned by the tool, in relation to a particular output, should be understood in the context of the above explanation. In reality, the waveforms (currents and voltages) in an InnoMux-controlled topology are characterized by patterns, incorporating pulses of energy delivered to different outputs and the transient processes associated with the switching of the energy delivery from one output to another. Consequently, the initial conditions at the beginning of two consecutive switching cycles are not necessarily the same, and current continuity factor cannot be defined in the conventional sense. The requests for energy delivery depend on the loading conditions and load combinations in the converter. These requests arise asynchronously. Thus, the switching patterns vary continuously. Therefore, the numerical results from the tool (frequencies, currents, cont. factors etc.) should be viewed as long term averages, rather than instantaneous or cycle values (peak, average or RMS) of the electrical quantities they represent.

The tool implements the fundamental requirement for a InnoMux transformer to ensure graduated primary reflected output voltages (Equation 1). The second fundamental InnoMux requirement implemented in the tool is that the output with the highest voltage should always operate in DCM. Both requirements result in the possibility that under certain load and line conditions, at least one of the remaining outputs may operate in CCM. See Figure 8 below.

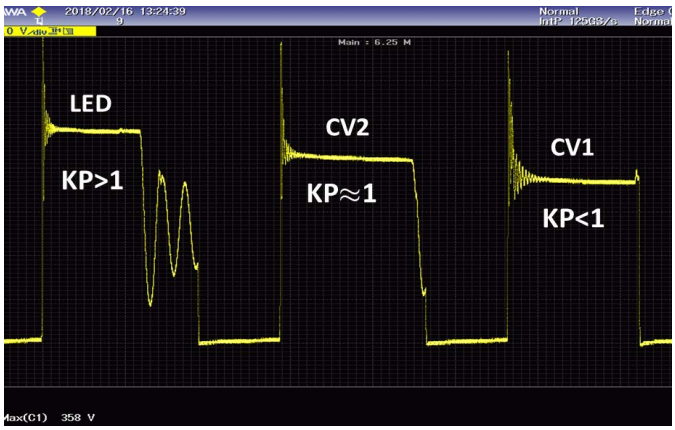

Figure 8. Primary Switch Drain Voltage of a Three-Output InnoMux Flyback Converter.

The tool implements worst-case (WC) tolerance design. Two input variables are subject to tolerance calculations: the transformer primary inductance LP and the primary current limit I_{LIMIT}. The former tolerance is user selectable, whereas the latter is fixed in accordance with the InnoSwitch3-MX data sheets. The tool calculates LP value such that at full power, at the minimum of the input DC rail and in the WC tolerance combination, the second InnoMux requirement is met. As a result, if a converter is built with nominal LP and I_{LIMIT}, it will operate further in DCM than anticipated. The tool does not take into account the tolerance of the input filter capacitor(s). It is up to the user to include it in the design input. For details on how to use the InnoMux PI Expert online tool, please also consider PIXls Application Note PI-41291787.

Design for Best Efficiency

The large part of the power dissipation in an InnoMux converter is in the primary switch and the transformer. Importantly, these devices do not lend themselves easily to heat sinking. Therefore, minimizing the losses in the primary switch and the transformer is important both for improving the converter efficiency and for its thermal performance.

The switching loss in the primary switch is dominant. The full power switching frequency needs to be kept low. A primary switching frequency in the range of 60 kHz – 70 kHz is usually a good initial choice. Lower frequency values may lead to increased audible noise as the power is multiplexed between the outputs.

Low reflected voltage VOR and low peak current I_p will reduce the switching loss in the primary switch. Under assumptions 1) and 2), the minimum reflected voltage of the CC channel is related to the primary peak current Ip according to the equation:

$$VOR_{MIN}CC = \left(\frac{I_P}{2 \times PO_{TOT}} - \frac{1}{VMIN} \right)^{-1} \qquad \text{Equation 4}$$

where V_{MIN} is the minimum DC input voltage. The equation shows that the VOR can be minimized by increasing I_P. If the frequency is to

remain the same, this can only be accomplished by selecting a primary device with higher I_{LIM}. This will have additional benefit of reduced $R_{DS(ON)}$. Low VOR also means that the reverse voltage across the rectifiers will be relatively high. This will necessitate the use of devices with high voltage ratings and high forward voltage V_F, which will increase the secondary conduction loss. The trade off between VOR and rectifier voltage rating often needs to be verified experimentally. Otherwise, the selection criteria for rectification devices in an InnoMux-controlled converter are no different from those of any other flyback converter.

In order to minimize transformer core loss and audible noise, the peak flux density of 220 mT or lower is recommended at full power. The transformer construction requirement in InnoMux converters is the same as it is in a conventional flyback converter. In order to minimize overspill, interleaved windings with low leakage inductance are recommended. A two-section primary winding with all secondary windings sandwiched between them is a good practice.

The losses in the InnoMux device are usually benign and no special cooling arrangements are necessary. The voltage(s) at the CHANNEL (ICC) pins are minimized by the control loop in order to minimize the loss in the CC drivers. The most common cause for increased power dissipation in the device is when the voltage on the OUTPUT VOLTAGE (VCV2) pin is left below its minimum required level $V_{CV2(MIN)}$. In such situation the device will derive its power supply from the OUTPUT VOLTAGE (VLED) pin, which results in increased loss in the internal voltage regulator. See section 2.4.

Audible Noise Reduction

There are three main sources of acoustic noise in a transformer:

- Vibrations of windings due to magnetic forces acting on the winding,
- Vibrations of the core due to magnetic forces, and
- Change of the core dimensions, i.e. magnetostriction.

The first of the three sources is thought to have only a benign contribution, easily eradicated by arresting the movement of the bobbin in the transformer/PCB assembly mechanically (gluing and/or varnish impregnation of the winding etc.). The effect of the remaining two sources of acoustic noise could be suitably mitigated both in the magnetic design and in the manufacturing process of the transformer.

Reduced Peak Flux Density B_M

Below the magnetic saturation point of the core, both the magnetostriction and the forces between the two core parts depend on the square of the magnetic flux density $B^2(t)$. Consequently, if the converter switching frequency is in the audible range or if a low-frequency mechanical resonance is excited, the resulting sound pressure level (SPL) will be itself a function of the ac component of $B^2(t)$. Figure 9 and Figure 10 show normalized $B^2(t)$ time-function and its harmonic content for a discontinuous flyback converter.

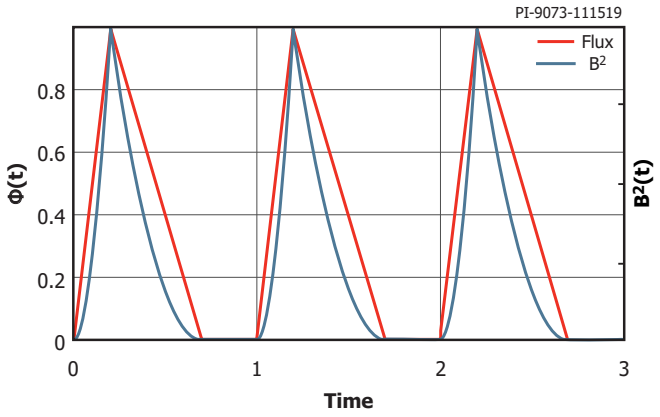

Figure 9. Normalized Magnetic Flux Φ(t) and Flux Density Squared $B^2(t)$ for a Discontinuous Flyback Converter.

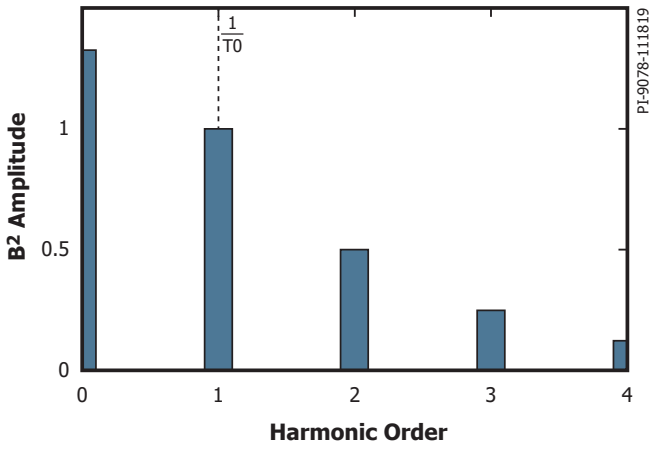

Figure 10. Discontinuous Flyback Converter $B^2(t)$ Harmonic Content.

One obvious way of reducing the SPL is to minimize the operating peak flux density in the core (B_M). In most cases full power B_M of 220 mT or lower results in relatively quiet transformer. This has the additional benefit of reducing the core loss. However, a core with larger magnetic cross section A_E and/or larger window will be required.

Increased Full Power Primary Switching Frequency

The total output power of a flyback converter is a square function of the primary peak I_p current and a linear function of the switching frequency f_{SW}. In an InnoMux controlled flyback these two quantities are related according to the curve shown in Figure 11. It is evident from Figure 11 that for a given primary inductance L1, as the overall power demand reduces, both the f_{SW} and I_p (i.e. B_M) will decrease. It is therefore desirable to choose relatively high full-power primary switching frequency f_{SW}, so that the power (hence $B^2(t)$), can be reduced significantly before the switching frequency becomes audible.

There are two main limitations in increasing f_{SW}.

Increased f_{SW} results in lower efficiency (i.e. higher core loss, copper loss and primary switch loss). InnoSwitch3-MX and in most cases the transformer are not designed for heat sinking and increased loss in these components may result in increased operating temperatures.

Where a WC tolerance design is required a converter built with nominal component values will have much lower primary switching frequency f_{SW} than desirable, in order the WC highest $f_{SW(MAX)}$ to remain inside the frequency control range of the controller.

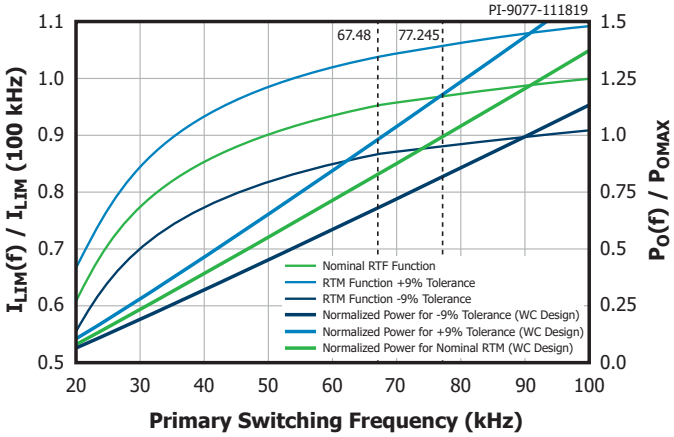

Figure 11. InnoSwitch3-MX RTM Curve.

Example: A 75 W converter is designed based on I_{LIMIT} tolerance of ±9% and primary inductance L1 tolerance of ±10%. At full power WC highest primary switching frequency $f_{SW(MAX)}$ is 100 kHz; the nominal primary switching frequency f_{SW} is 79 kHz and the WC minimum frequency $f_{SW(MIN)}$ is 64 kHz. In this case f_{SW} = 79 kHz is as high as the nominal primary switching frequency can be. If the converter was designed for f_{SW} > 79 kHz, then $f_{SW(MAX)}$ would fall outside the controller frequency range and in the WC tolerance combination the controller would run out of regulation. This limitation is even more severe if any of the outputs needs to operate in CCM.

Low Reflected Voltage Differential

As illustrated on Figure 8, for the correct operation of an InnoMux controlled flyback converter, there should be a differential between the primary reflected voltages of the individual outputs (Equation 1). This means that the flux Φ(t) in the transformer core will decline at a different rate depending on the output being charged. This in turn will change the harmonic content of the $B^2(t)$ function. An example of a two-output converter is shown in Figure 12 and Figure 13. It is evident that the difference between the reflected voltages of the two outputs generates harmonic content in the $B^2(t)$ function below the primary switching frequency. Consequently, as the power demand is reduced down from its full-power level, the transformer will become audible at higher powers compared to the converter illustrated on Figure 10. To reduce the energy in the low frequency harmonic content the difference between the reflected voltages of the individual outputs should be minimized. Indeed, Figure 9 and Figure 10 indicate that no low frequency content is generated if the two outputs have the same VOR. Unfortunately, the difference in VOR of the individual outputs cannot be set to zero. It needs to be sufficient for the correct operation of the InnoMux converter (Figure 8). Moreover, in most applications the CC output is required to operate in a wide voltage range.

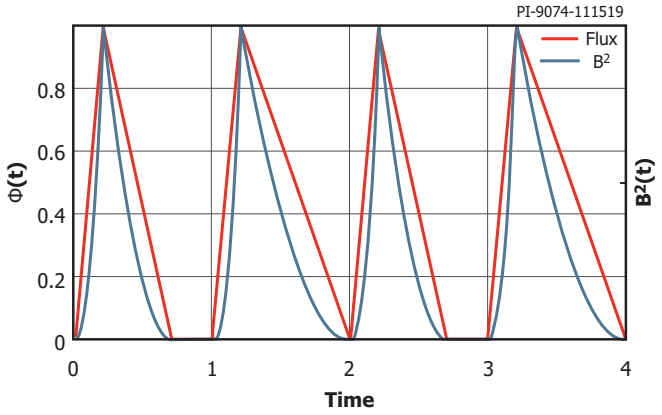

Figure 12. Normalized Φ(t) and $B^2(t)$ for a Two Output InnoMux Flyback Converter. (VOR1 ≠ VOR2)

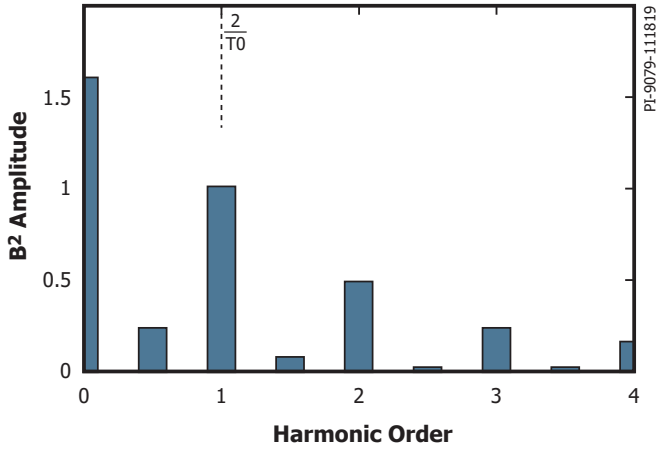

Figure 13. Two Output InnoMux Flyback Converter (VOR1 ≠ VOR2) – $B^2(t)$ Harmonic Content.

Even if the transformer is designed to produce minimum VOR difference for the lowest LED voltage, this difference will increase as the LED voltage increases up the range. It is therefore not advisable in LED monitor applications, that a range of LED panels is covered by too few PSUs, because each PSU will have to cover wide range of LED voltages.

Generally, the switching pattern of an off-line InnoMux converter is determined by its operating point in terms of total power, output loading combination and input voltage. There may be up to 3 outputs sharing the total power in an infinite number of combinations. The converter operating point translates into a set of output request frequencies, governing the switching pattern. The energy requests from the converter outputs arise asynchronously. Therefore, the switching patterns are continuously variable with line and load. Furthermore, the CC output always operates in DCM, whereas the CV outputs could operate in both CCM or DCM. Consequently, the secondary conduction intervals, the current continuity and the number of consecutive pulses delivered to any one output are different for different outputs and depend on the power delivered to the output. Hence, primary peak current I_p and conduction interval vary too. Figure 14 and Figure 15 illustrate the full power operation

of a 1 × CV + 1 × CC outputs Flyback converter, where the power requested by the two outputs is in such proportion that it is necessary to deliver two consecutive pulses to the lower voltage (CV) output for each pulse delivered to the higher voltage (CC/LED) output. Also at low line the CV output operates in CCM.

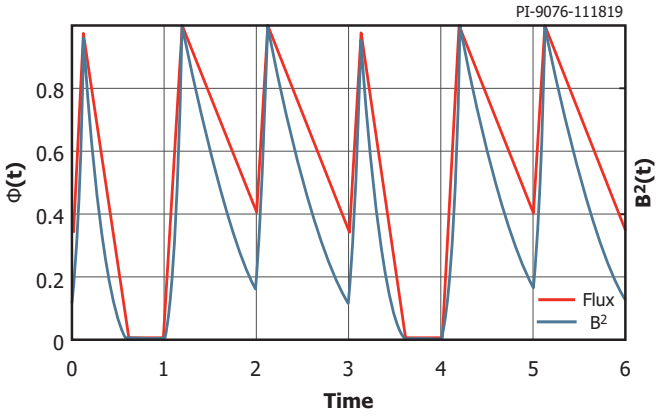

Figure 14. Normalized Φ(t) and B²(t) for a Two Output InnoMux Flyback Converter. (VOR1 ≠ VOR2; CC – DCM, CV – CCM)

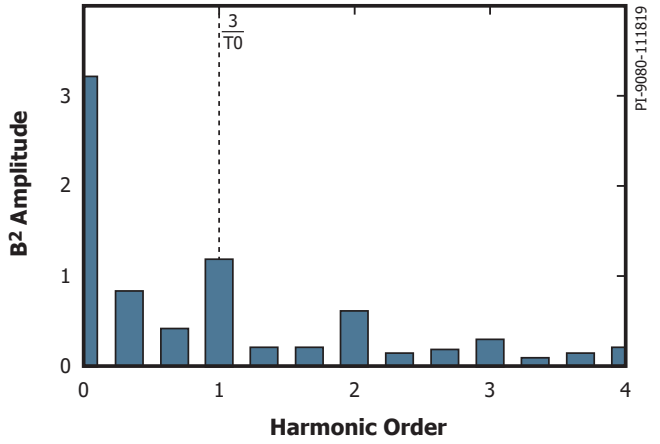

Figure 15. Two Output InnoMux Flyback Converter B²(t) Harmonic Content (VOR1 ≠ VOR2; CC – DCM, CV – CCM).

The switching patterns in Figure 9, 10, 12 to 15 illustrate specific loading combinations of a two-output InnoMux converter. In reality, the B²(t) function is much more complex than suggested by these illustrations. Consequently, its spectrum will contain a multitude of components below the switching frequency with different amplitudes. The presence of these components will be reflected in the resulting SPL. To an extent, the scattering of the acoustic pressure in wider frequency spectrum lessens the subjective perception of noise, compared to a case where it is carried by a single tone (frequency).

LED Dimming Frequencies

InnoMux controllers feature a number of PWM dimming methods. Simple PWM dimming mode allows frequencies between 100 Hz and 27 kHz. Although the change in light intensity in this frequency range is not detectable by the human eye, the modulation of the LED current may generate audible noise in the transformer. It is therefore advisable to avoid the lower part of the PWM dimming frequency band if the application allows it.

Using Appropriate I_{LIMIT}

It is important that a primary switch (InnoSwitch3-MX) with appropriate current limit (I_{LIM}) be used in a design. The transformer needs to be designed for this particular I_{LIM}. Changing the primary device retrospectively without re-designing the transformer could result in acoustically noisier operation. In the 12 W converter example below the transformer was originally designed to operate with INN3464C I_{LIMIT} = 0.75 A. Subsequently, a larger device INN3465C was used with the same transformer. Since the transformer was designed with sufficient margin to saturation (B_M = 230 mT) the increase in I_{LIMIT} did not result in core saturation at full power. However, the acoustic noise levels were significantly different. In the latter case, the WC audible noise was about 9dB higher as illustrated on Figure 16 and Figure 17 below.

Figure 16. INN3464C – I_{LIMIT} = 0.75 A; VIN = 115 VAC; CV1: 5 V / 0.6 A; CC: 38 V (Worst-Case).

Figure 17. INN3465C – I_{LIMIT} = 1.15 A; VIN = 115 VAC; CV1: 5 V / 1.2 A; CC: 38 V (Worst-Case).

Transformer Manufacturing

It is important that the two core halves are fastened firmly and glued together on the side of the outer limbs. The transformer should be vacuum impregnated with varnish or other suitable compound and then dried.

PSU Assembly

The vibrations of the transformer can give rise to mechanical resonance, which amplifies a particular frequency of the audible noise it emits. The transformer itself will have a mechanical resonance frequency. The entire PSU assembly (or subassembly) may form a system with mechanical resonance, which could be excited by the vibrations in the transformer. The resulting vibration may be in the audio range. Care should be taken when fitting the transformer in the overall PSU assembly so that mechanical resonances are damped suitably. Also the PSU enclosure should not include openings causing sound refraction.

Other Sources of Acoustic Noise

Generally, components made of materials exhibiting electrostriction effect (eg. ceramic capacitors and low-quality filter-inductors) are also known to emit noise when subjected to switching frequency ripple. These components should therefore be avoided in the various loops with high ripple current.

Other Design Examples

https://ac-dc.power.com/der-636

https://ac-dc.power.com/der-871

Notes

Revision	Notes	Date
A	Initial release.	08/20
B	Corrected typo, added text on page 2 and updated Equations 1 and 3.	11/20

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Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza, No. 88
North Caoxi Road
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji Nan
8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

Germany (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

Germany (Gate Driver Sales)
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

Japan
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com